

# 19<sup>th</sup>. ESLS Workshop

# SESAME RF Status

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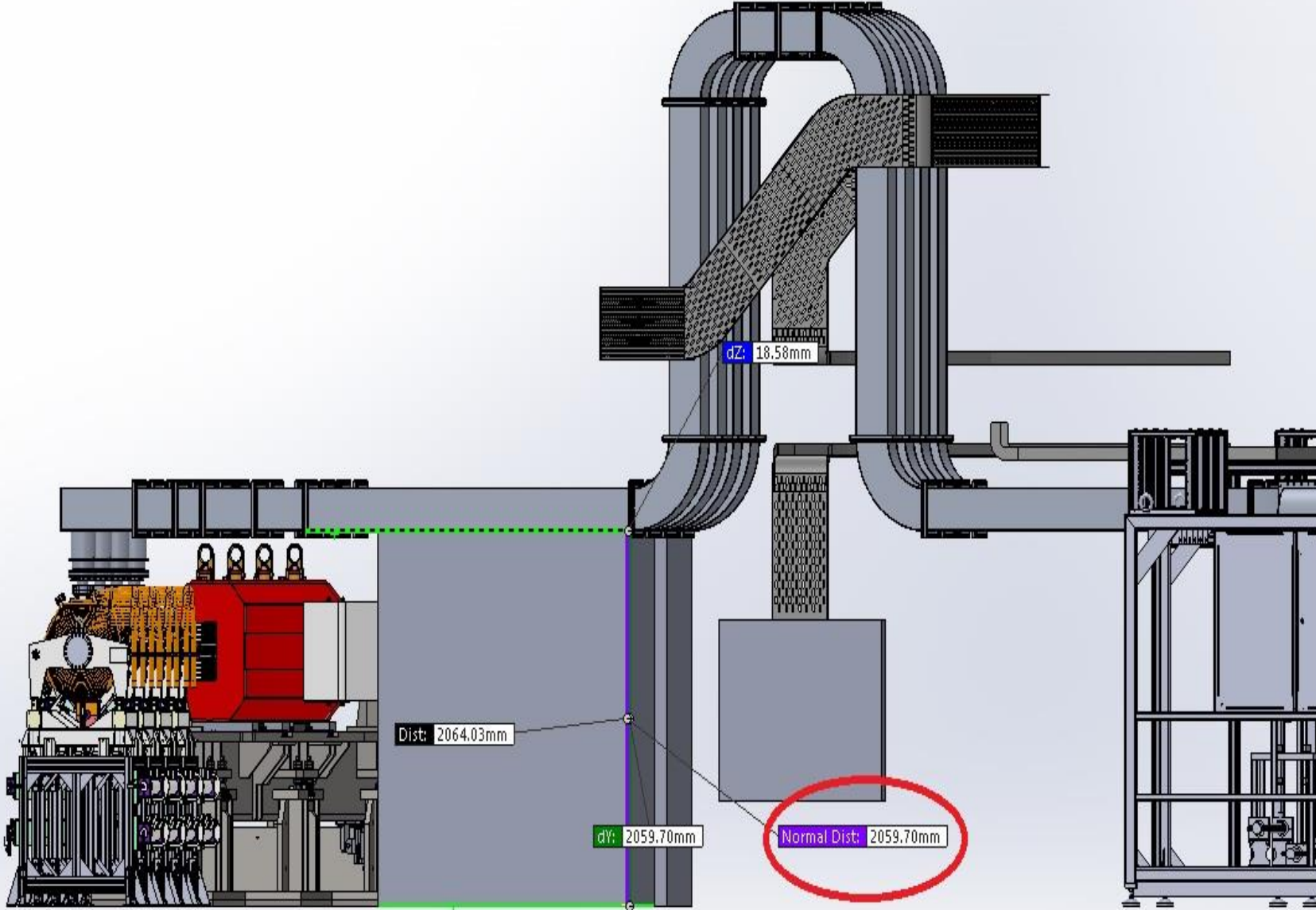
# The New Look of SESAME



# SESAME RF Plant

Aluminum Profile is used to carry the WG's

Proposed path of cable trays

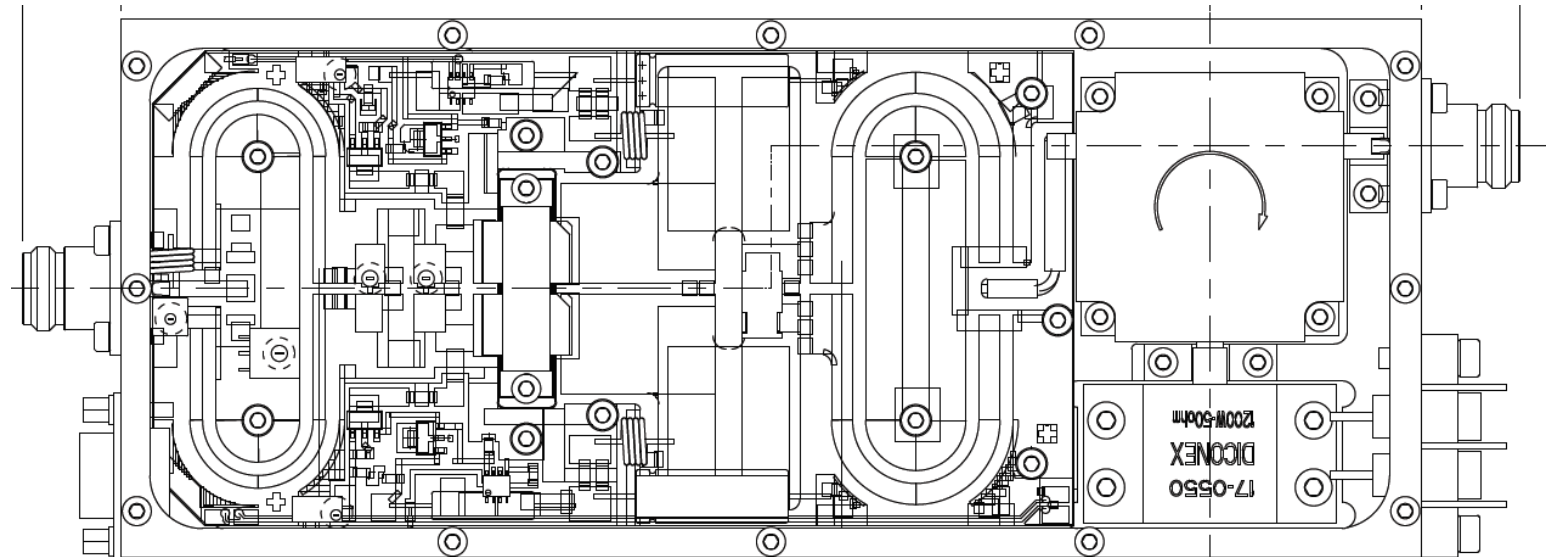
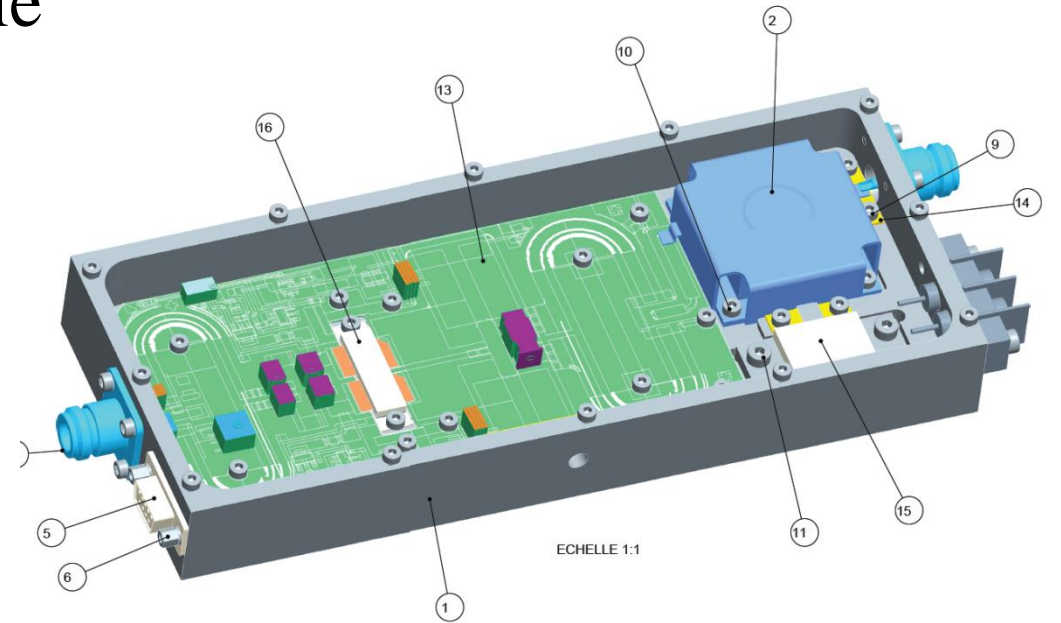


# SESAME SSA Module

## SEGMA-Phi modifications to SOELIL Design

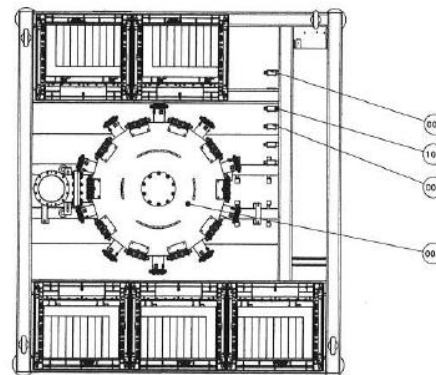
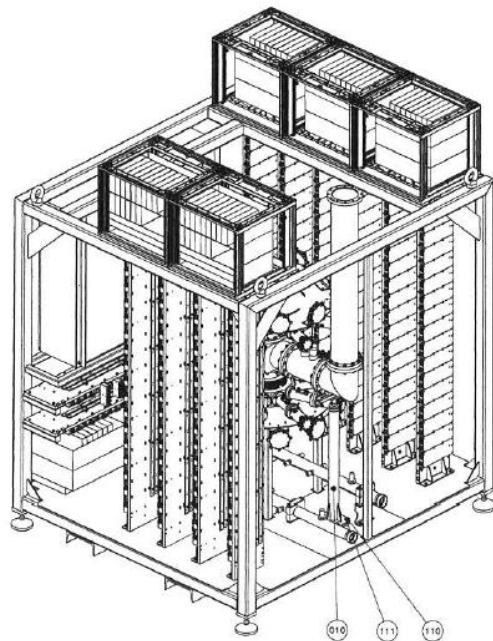
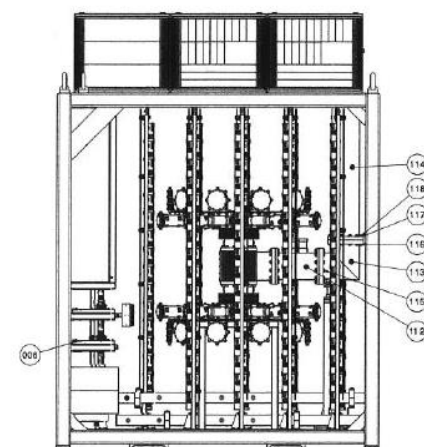
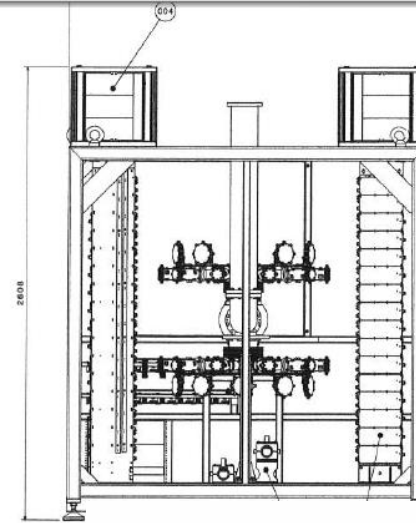
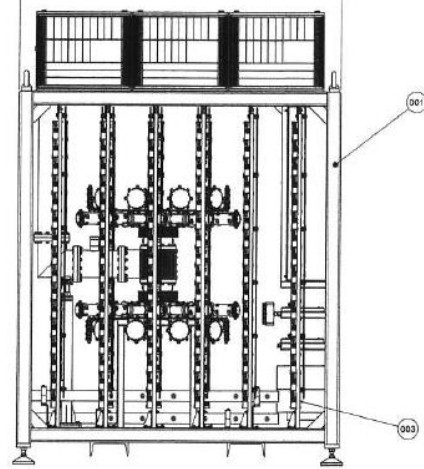
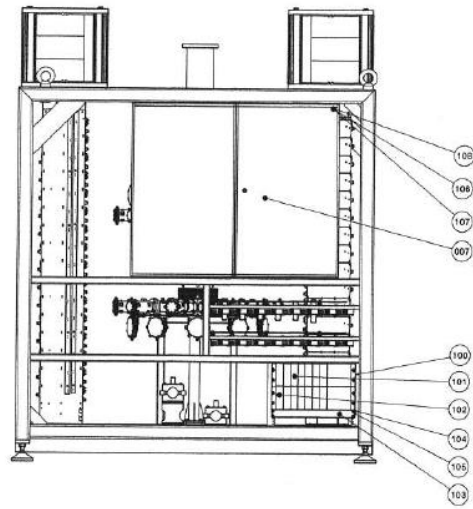
### New SESAME module:

- 2 PCBs added for circulator pins.
- Position of RF chokes.
- New SMD components.
- Output RF connector.
- Number of cover's screws.



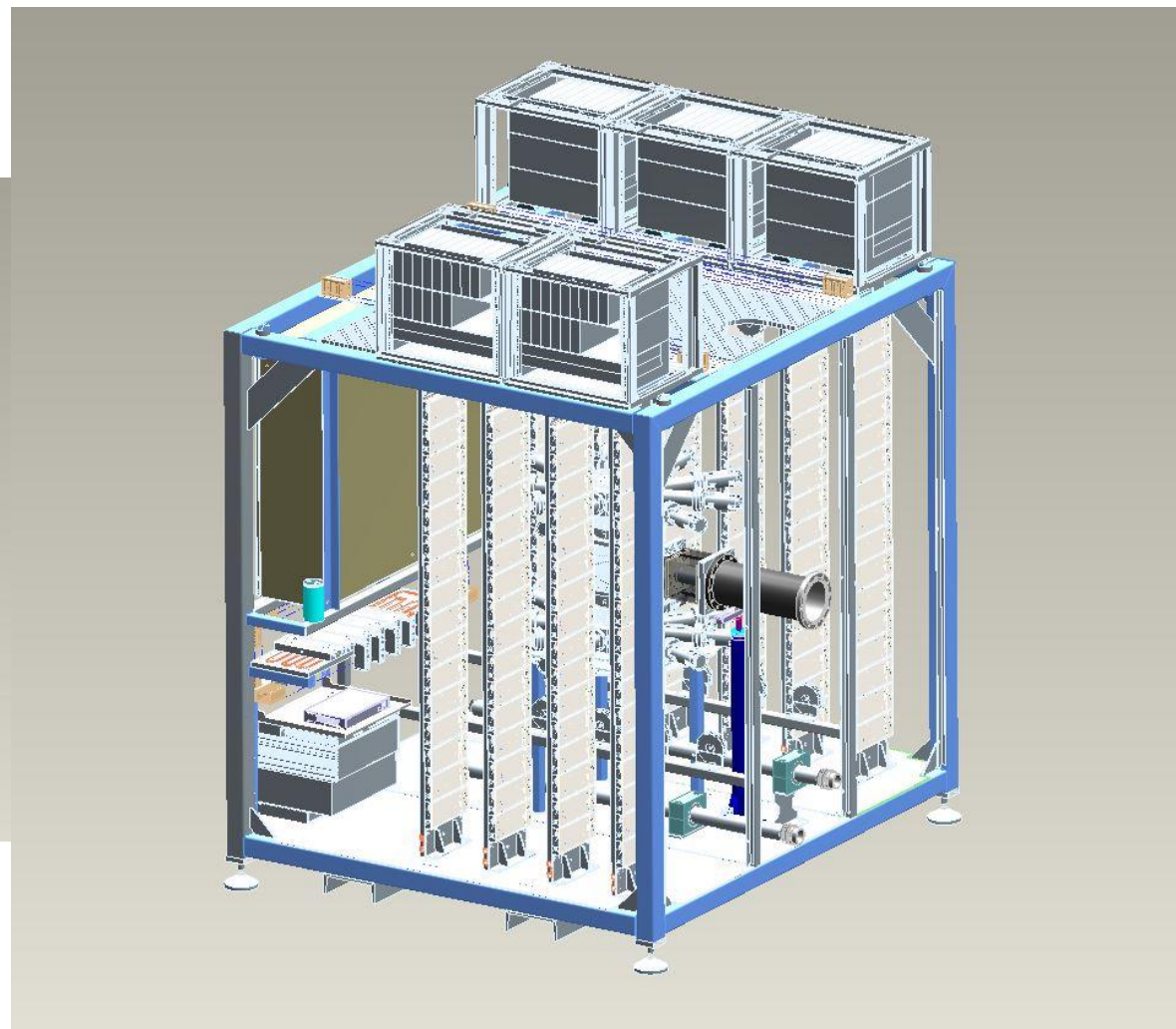
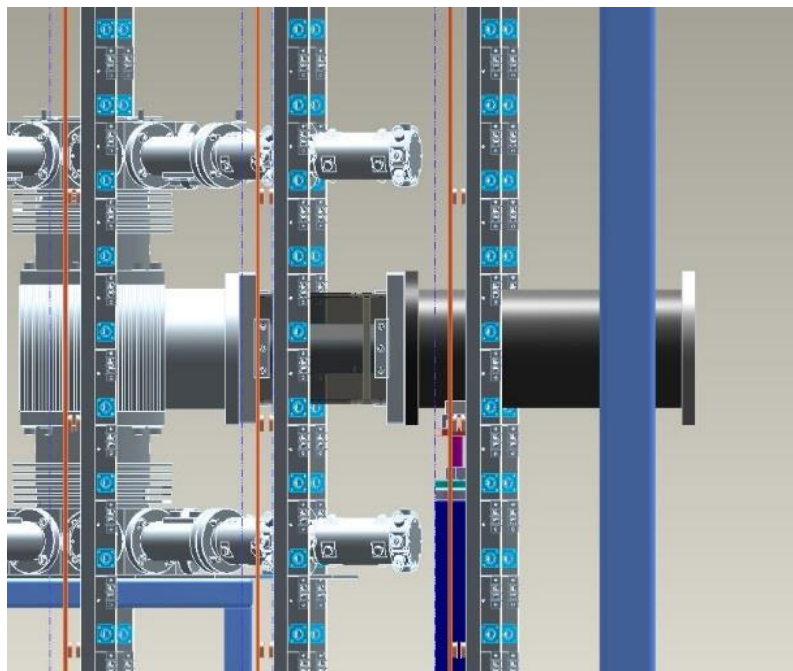
# The Old Layout of SESAME SSA

- One big concern regarding the length of the rigid coaxial with more than 1.5m which would face high VSWR creating more power than max. limit of coaxial.

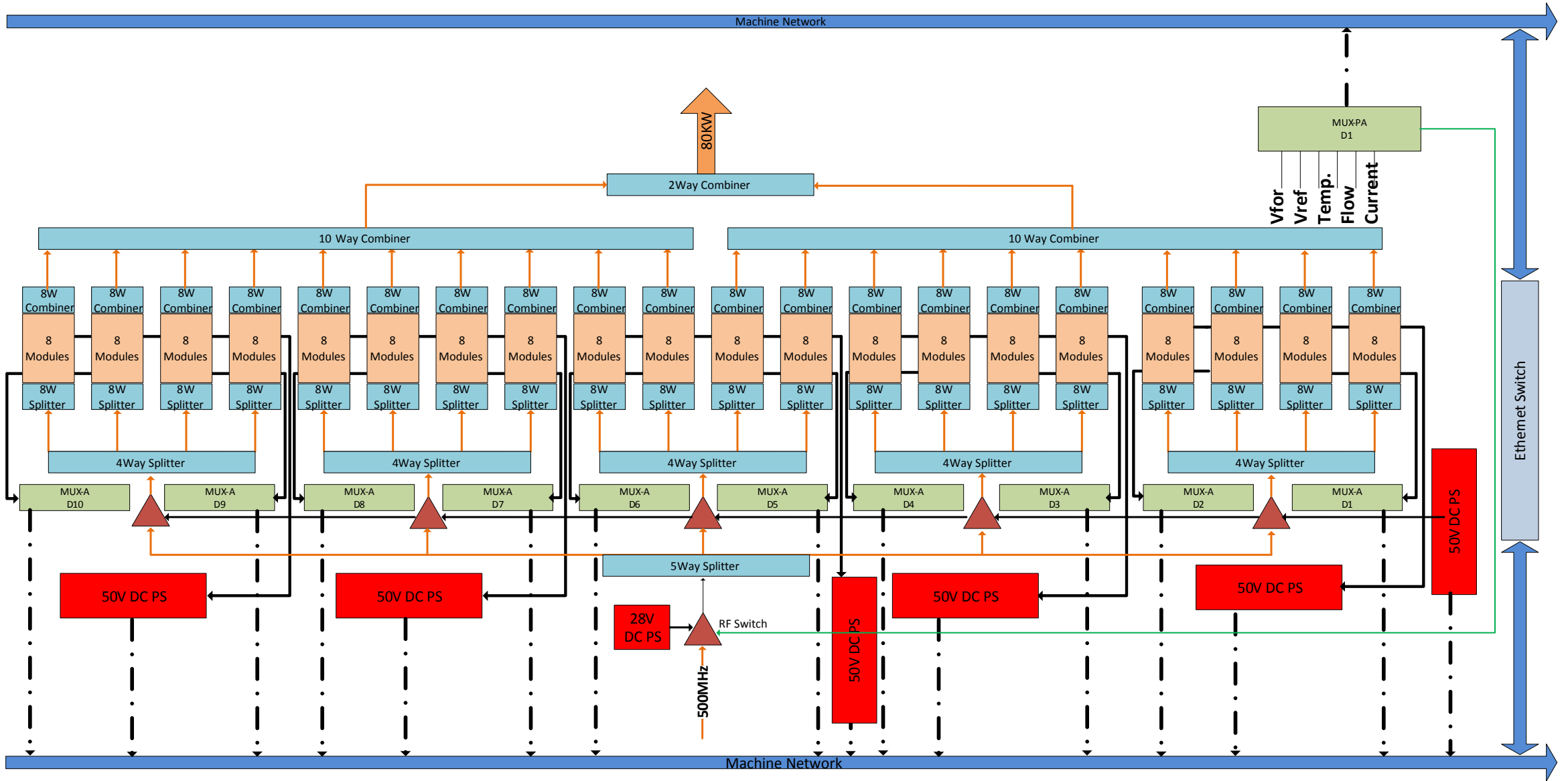


# SESAME SSA New Layout

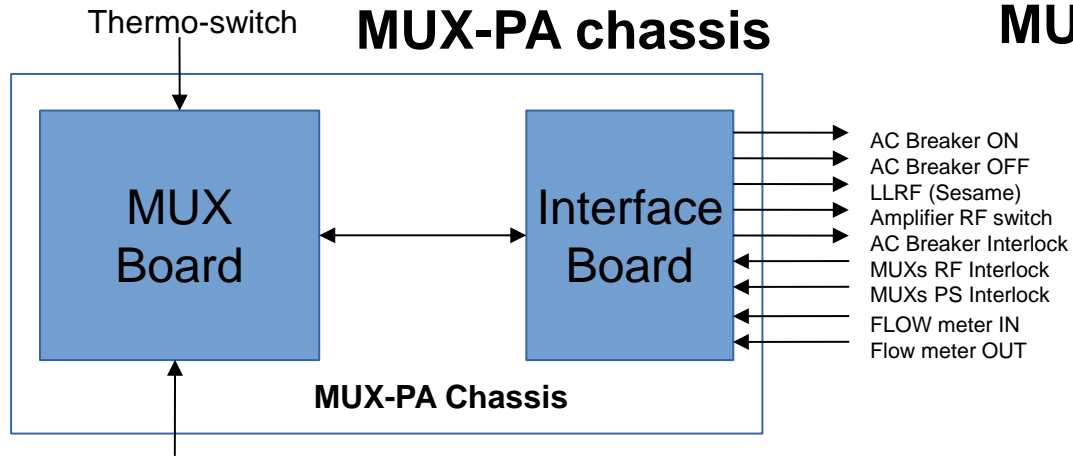
**Solution:** was by shortening the coaxial line to min and connecting the WG transition from the side.



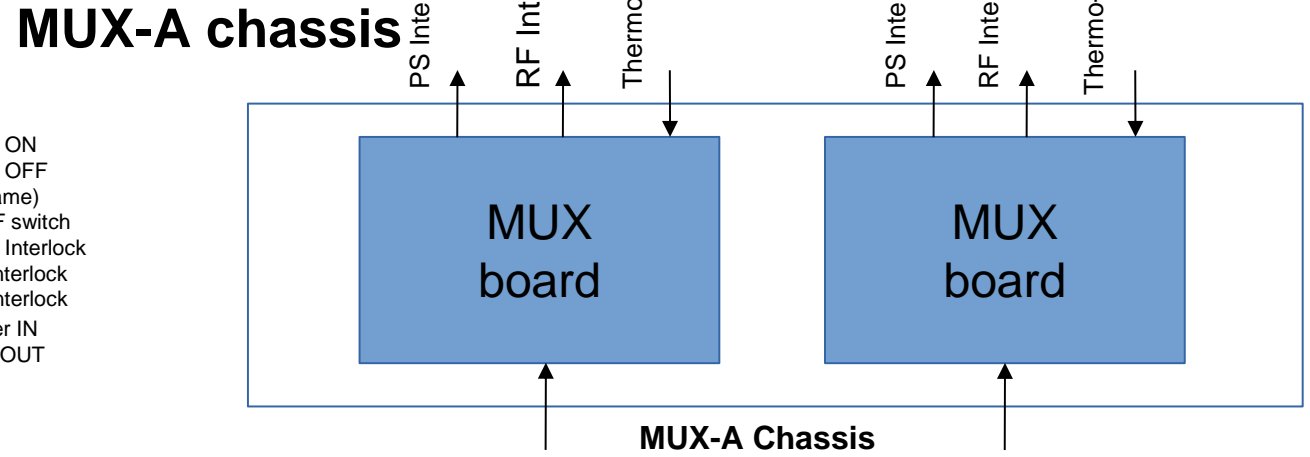
# SESAME SSA Architecture



# SESAME SSA Control System

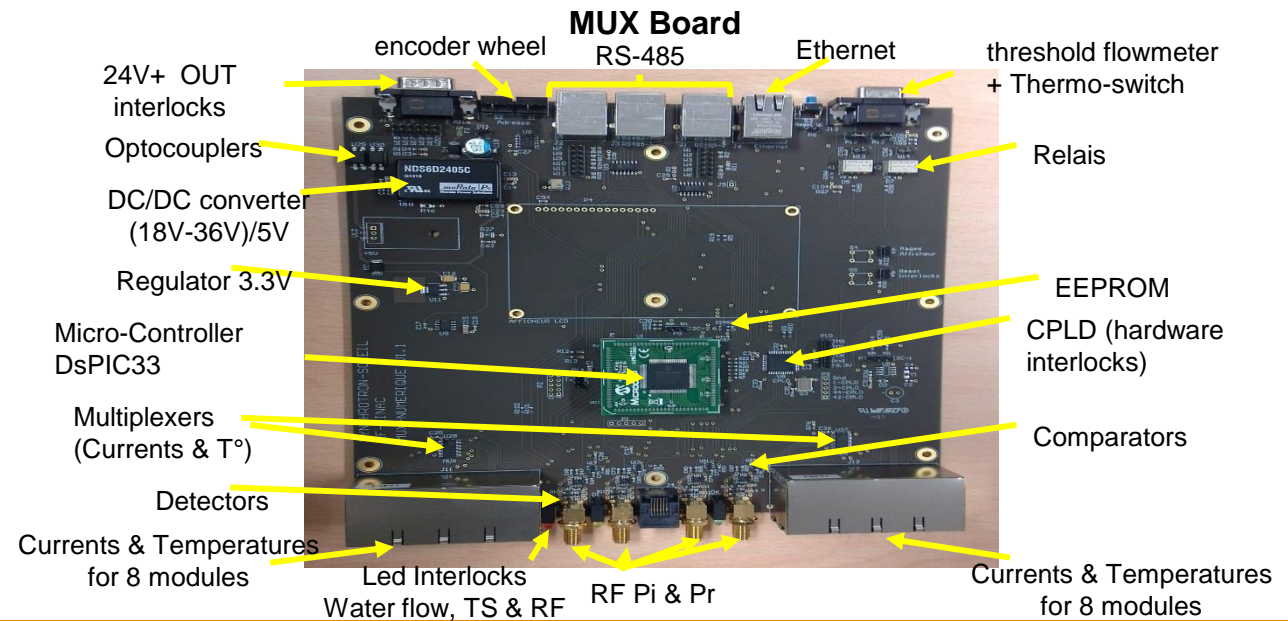
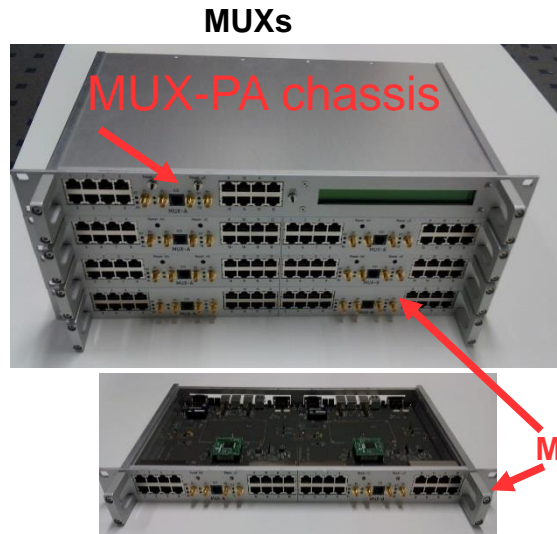


10 Currents, 5 Temperatures,  
4 RF Powers  
(5 modules of small dissipator)



32 Currents, 16 Temperatures,  
4 RF Powers (16 modules of 1 dissipator)

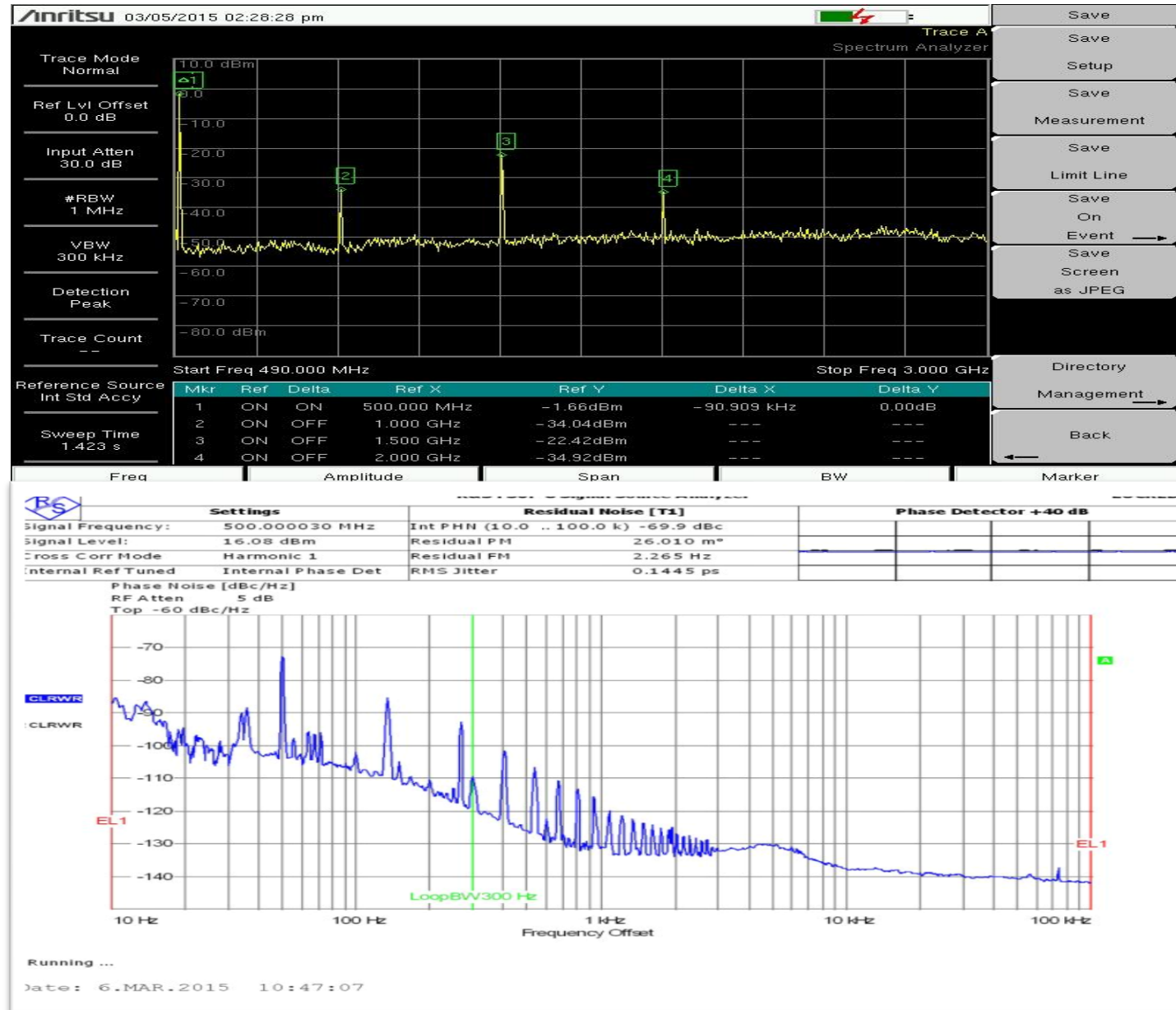
32 Currents, 16 Temperatures,  
4 RF Powers (16 modules of 1 dissipator)





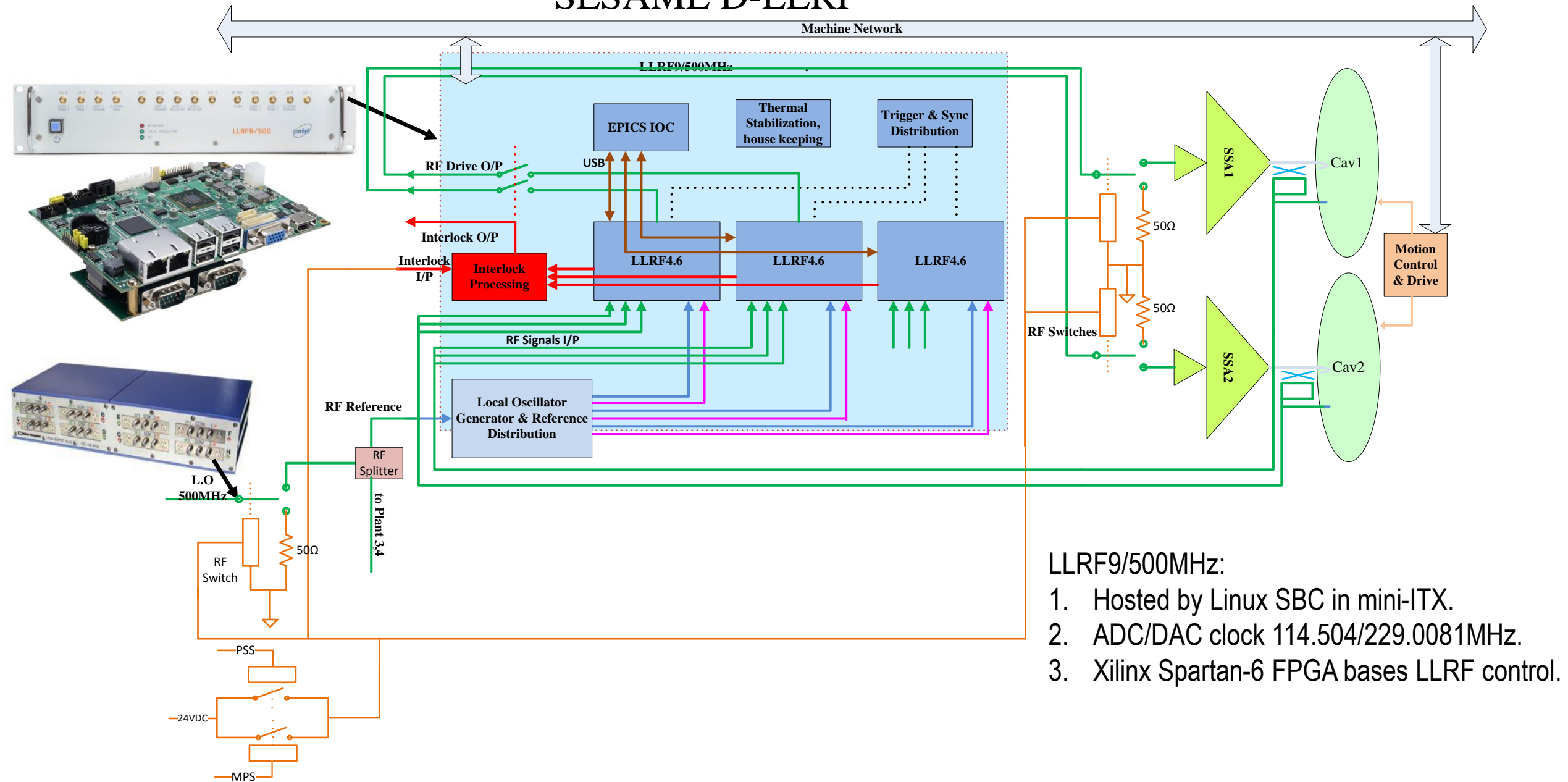
# Harmonics/Noise measurements based on THOMX SSA rack

- **Noise harmonics worst case is at 50Hz@-75dBc which is the AC line frequency.**
- **Distortion harmonics worst case is at 1.5GHz@-22.42dBm.**



# SESAME D-LLRF

Machine Network



LLRF9/500MHz:

1. Hosted by Linux SBC in mini-ITX.
2. ADC/DAC clock 114.504/229.0081MHz.
3. Xilinx Spartan-6 FPGA bases LLRF control.

# D-LLRF Specs & Features

Dimtel Features::

1. Amplitude, Phase and Frequency feedback loops Regulation

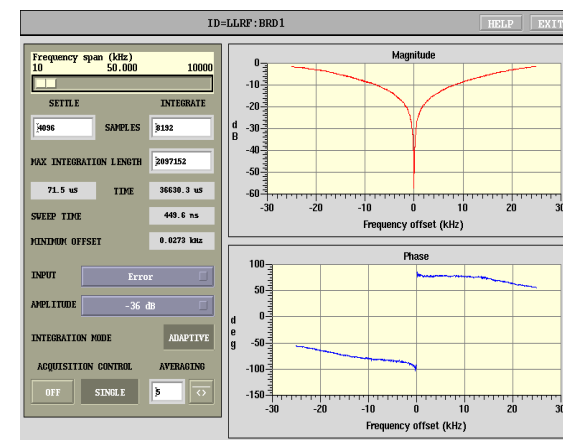
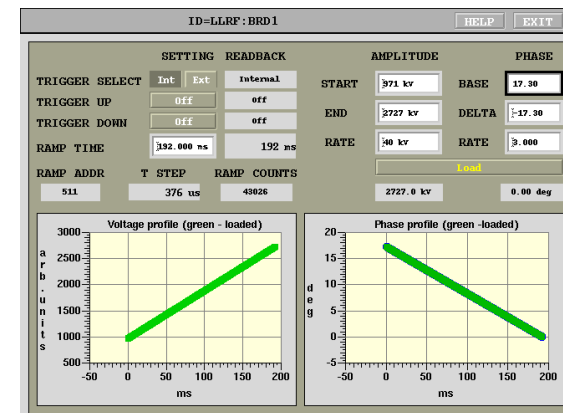
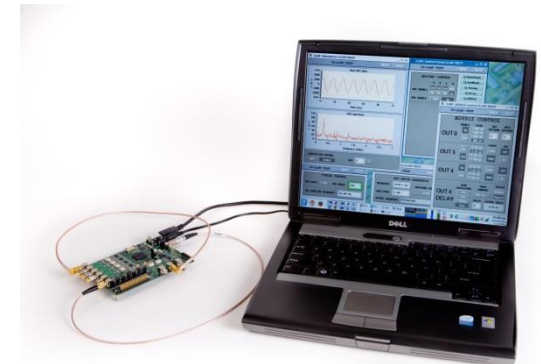
2. Diagnostics:

Time Domain

- Waveform Acquisition.
- Scalar Acquisition.

Frequency Domain Diagnostics:

- Real-Time Network Analyzer
  - Spectrum Analyzer.
3. Ramping pattern with period of 70us to 18.9s
4. S/ADC inputs requires current based sensors.
5. Open loops adjustments

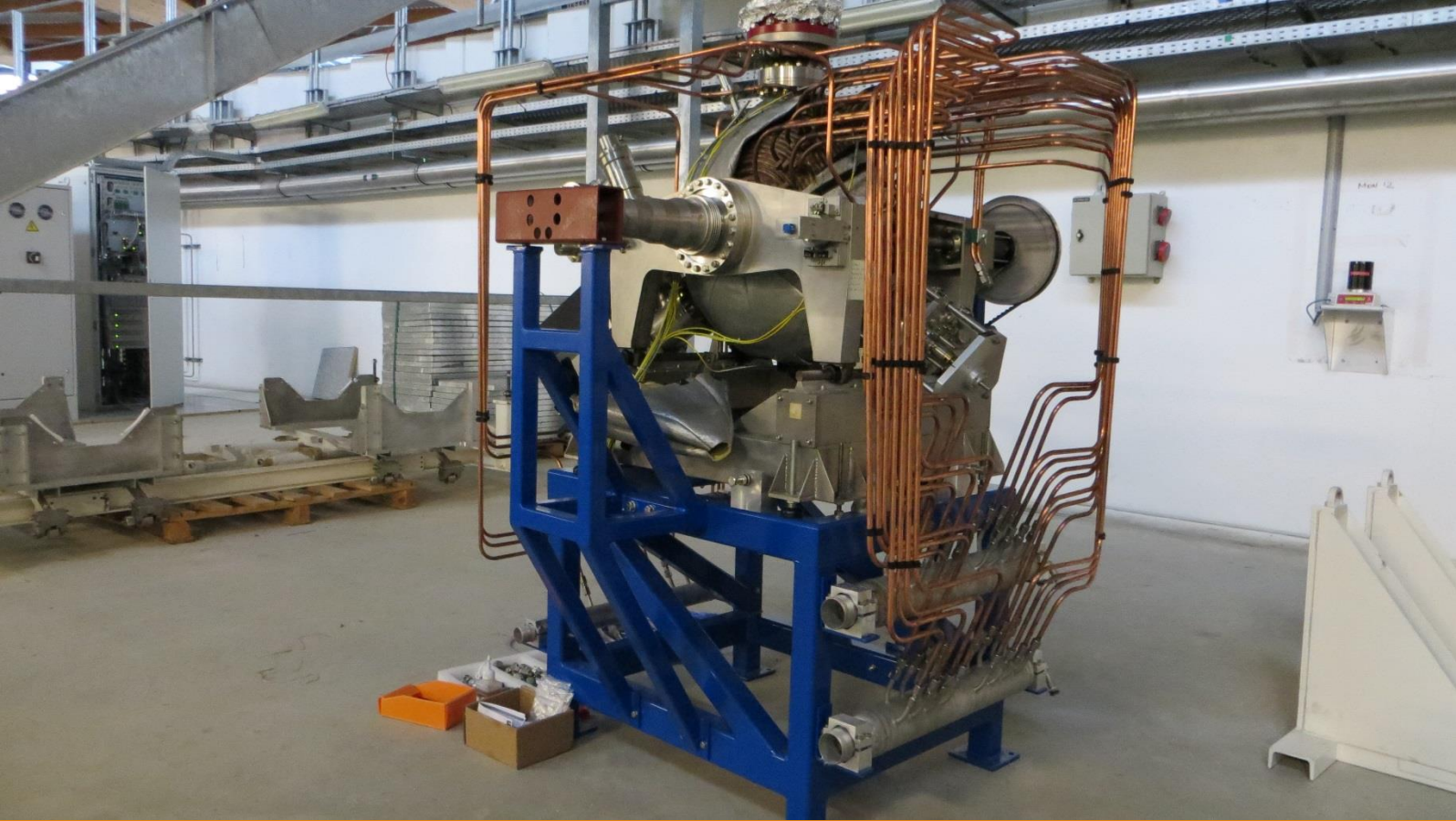


RF in	RF out	Amp Loop	Phase Loop	Freq. Loop	Processor	Slow ADC
9	2	<0.1%	<0.05°RMS			8
14bit @100MHz	14bit @100MHz	<b>BW</b> depends on the installation			IF: 41.6378 MHz F/ADC S. Rate: 114.504 MHz S/ADC S. Rate: 110 Ksps F/DAC S. Rate: 229.0081MHz	12bit
<+2dBm	>+3dBm	>40 dB	360°			



# SESAME RF Cavity

Assembled Elettra RF Cavity



RF Cooling Rack



# Manufacturing Process of Elettra Cavity for SESAME SR



Thank You

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