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The ISIS Synchrotron Digital Low Level RF System Upgrade

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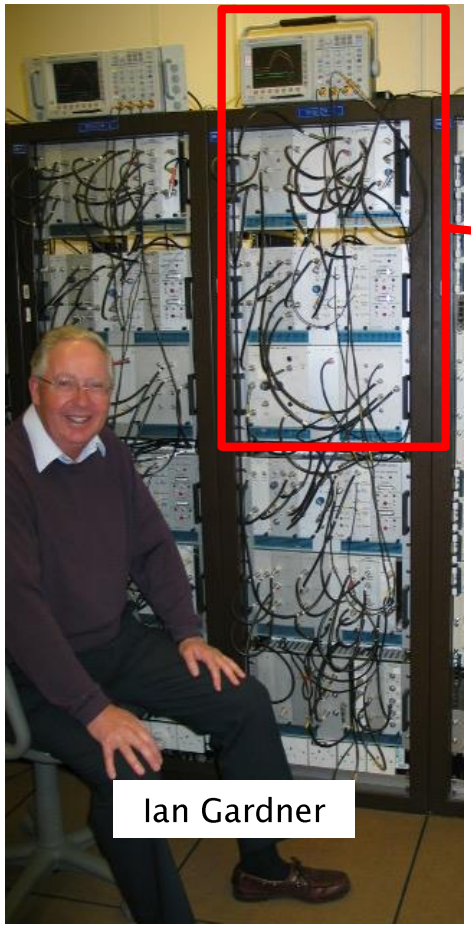
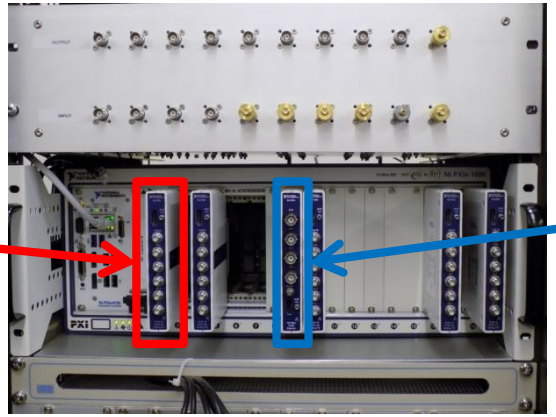
Acknowledgments





ISIS RF Team
Rob Mathieson
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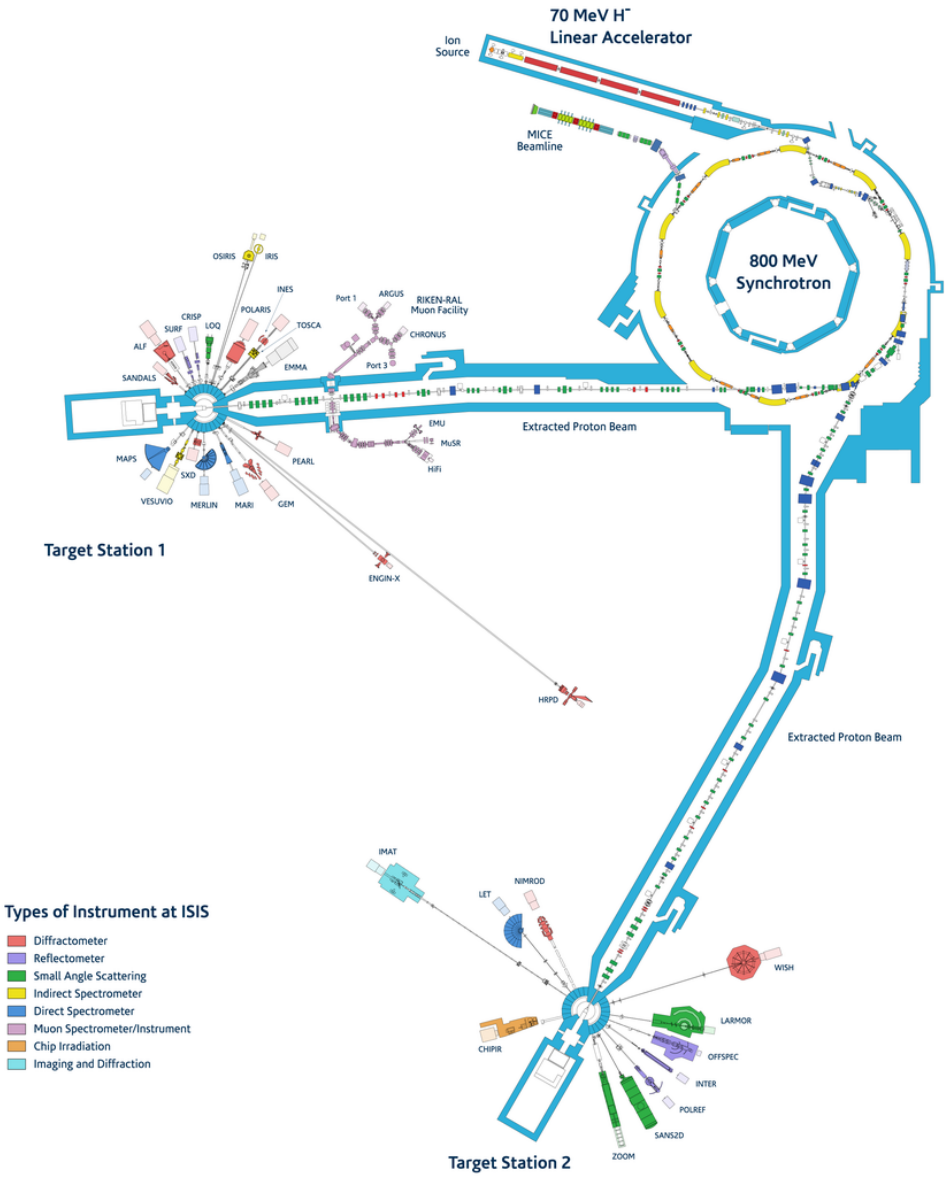
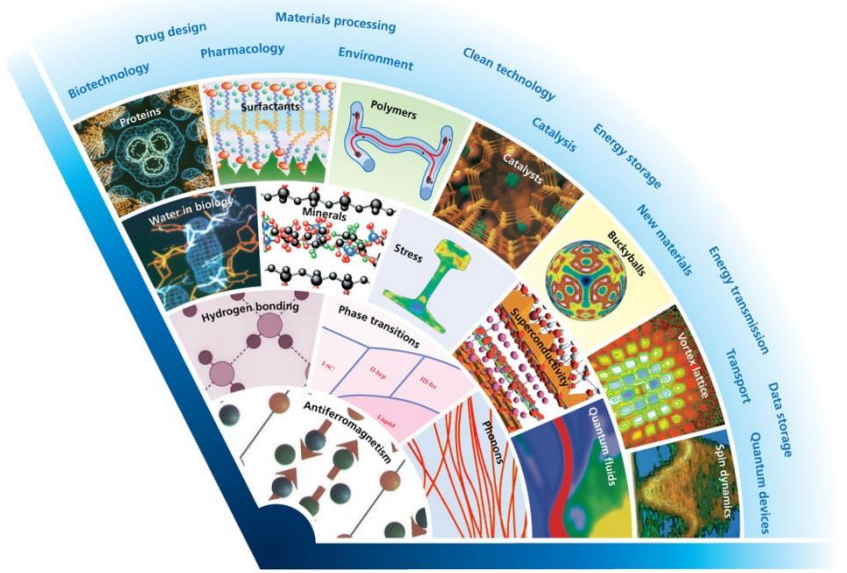
Ryan Allinson

ISIS Controls
Ivan Finch
Tim Gray
Gareth Howells

George Tsalavoutis (**NI**)

ISIS Neutron and Muon Source





More info @: www.isis.stfc.ac.uk

- First Beam to TS1Dec. 1984
- DHRF upgrade c.2000
- TS2 commissioned c.2009
- Now run >230μA beam current

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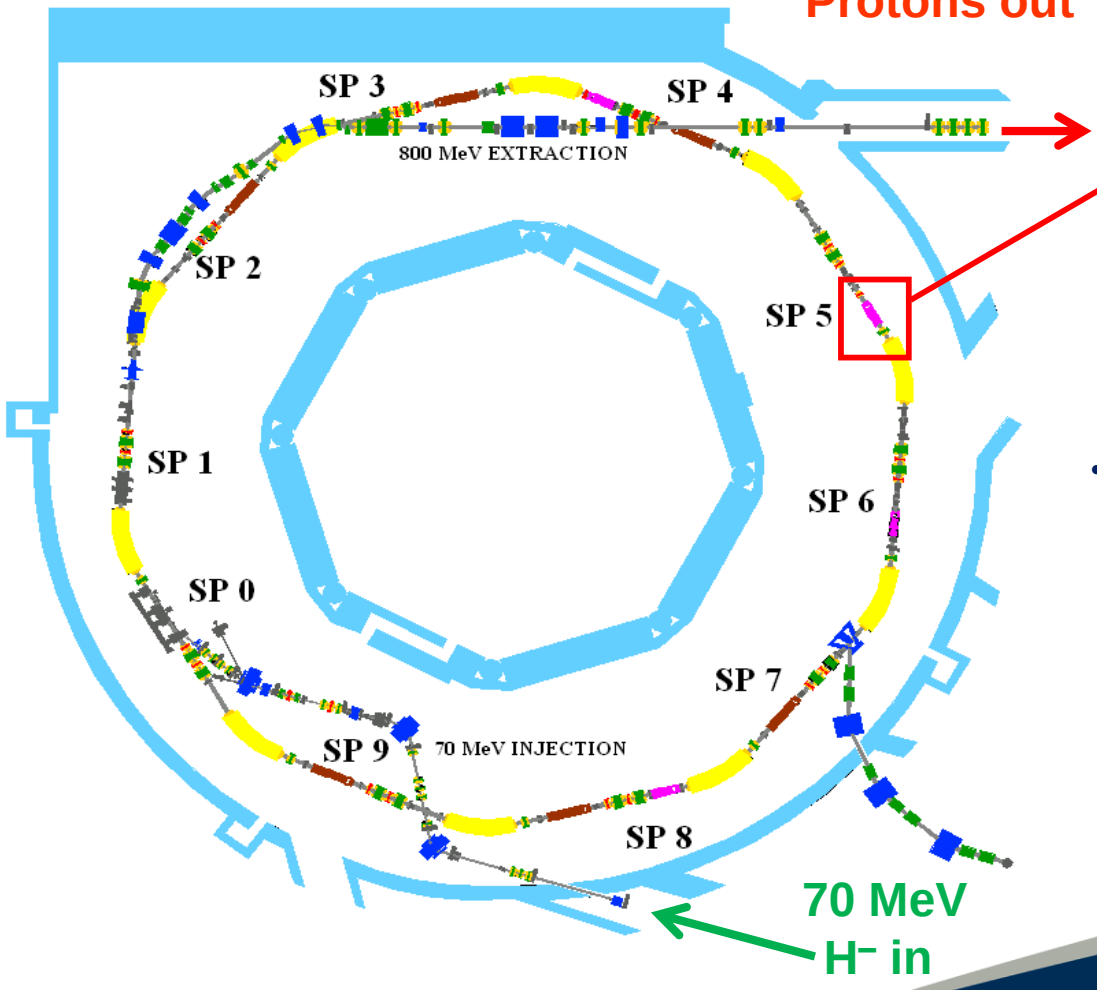
ISIS Synchrotron HPRF

- H^- ions stripped to protons when injected at 70MeV
- Protons complete ~12,000 turns in next 10 ms
- Accelerated to 800MeV
- Protons extracted & transported 2 targets
- Repeats @ 50Hz



- 10 x RF cavities provide electric fields to accelerate particles
  - 6 x 1RF (H=2) Cavities
  - 1.3-3.1MHz
  - 4 x 1RF (H=4) Cavities
  - 2.6-6.3MHz

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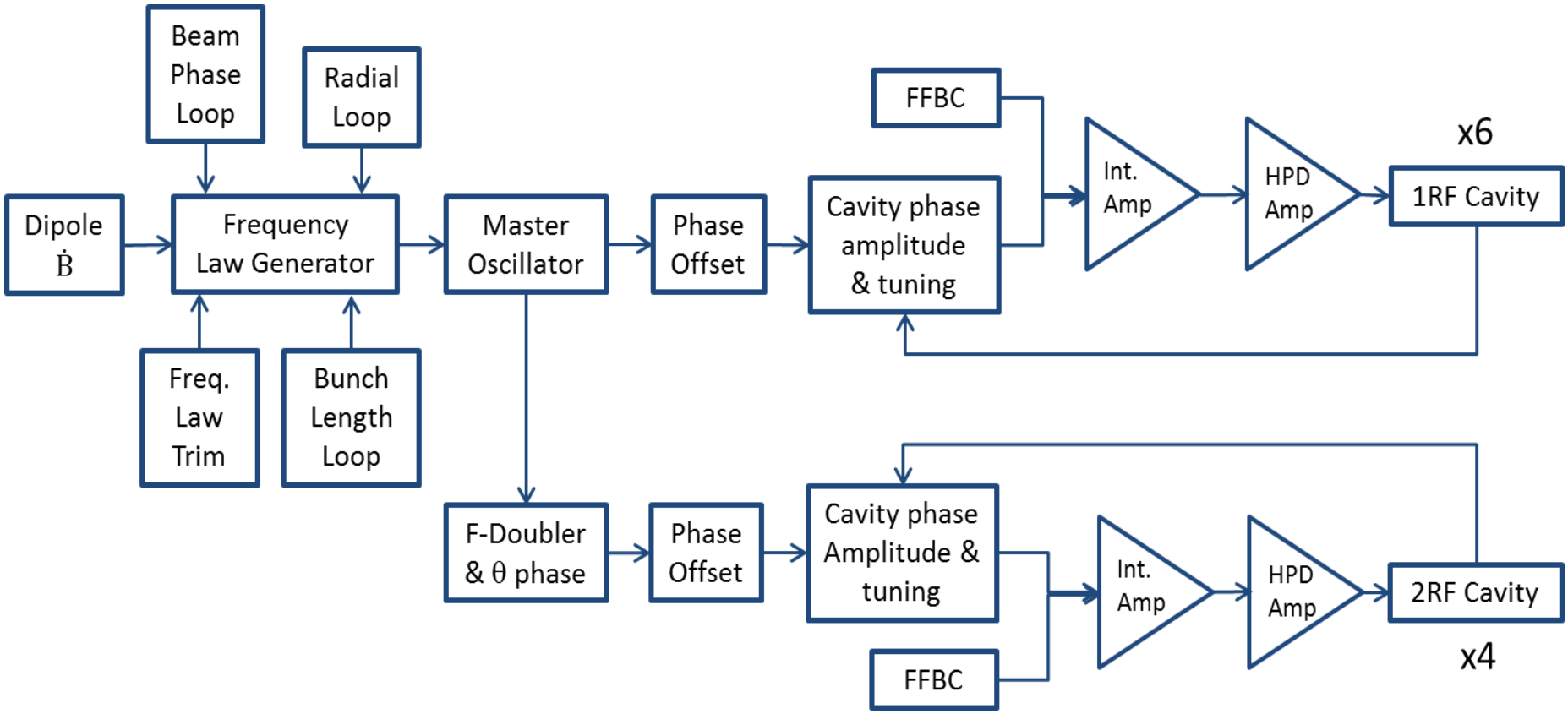
LLRF : System Overview



ISIS LLRF Controls (c. 2004)

Original (c. 1982)
Frequency Law Generator
/ Master Oscillator

Original 1RF Analogue LPRF controls (c.1982)

Loops to control cavity voltage amplitude and phase + tuning

2RF Analogue LPRF controls (c.1995)

Even the newer 2RF system ~10 years old.

- ageing components more likely to fail
- replacements harder to source

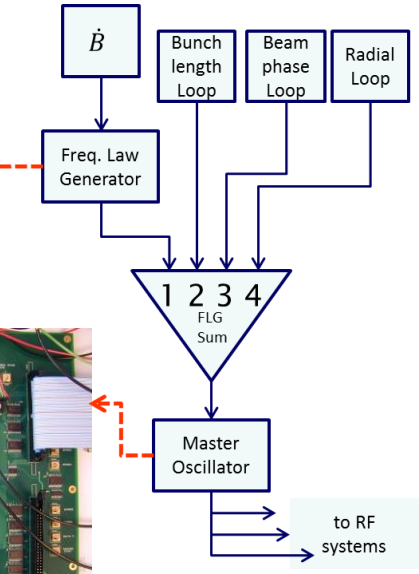
Time to think about replacing the system!

ISIS LLRF Upgrade – Potted History

~2005, started to consider replacements for the ageing LPRF controls:

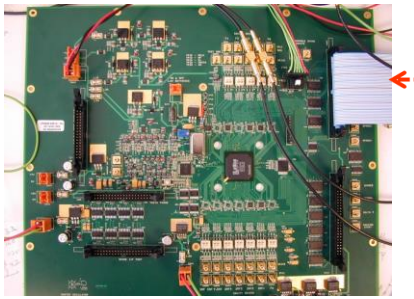
Frequency law generator:

- Lattice FPGA based
- Takes input Bdot signal and integrates to give current frequency.



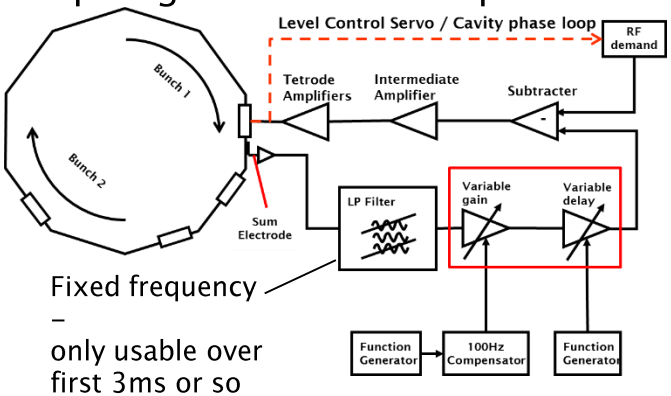
Digital Master Oscillator:

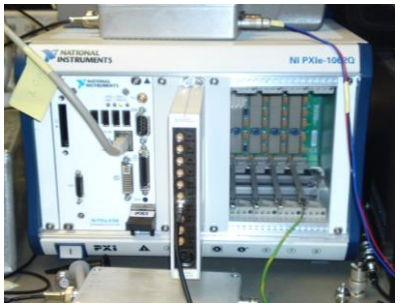
- Lattice FPGA based Voltage-to-Frequency Converter
- Provided RF signal to 10 Cavities :
  6 x 1RF, 4 x 2RF

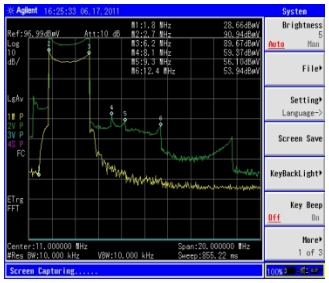


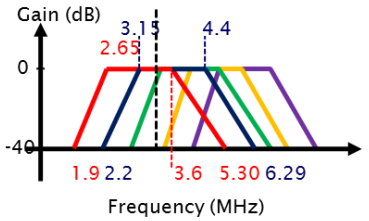
~2008 – Feed forward beam compensation

Swept digital filterbank implemented on New FlexRIO platform:



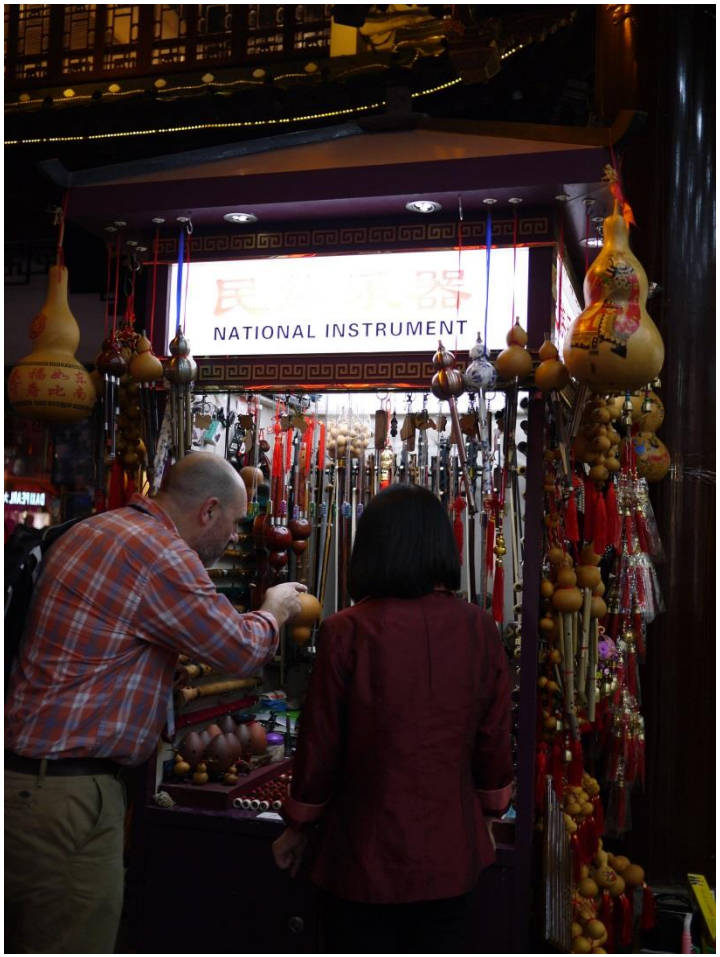






Why not use FlexRIO based system to replace LPRF controls?

NI FlexRIO – Digital LLRF



Choice of Platform

- NI global company
  - Large support network
- Use of LabView FPGA for coding
  - STFC has site licence agreement
  - Many LabView users / few VHDL
- Small team / Low channel count
  - off the shelf more cost effective
  - Less development time?
- Obsolescence less of a problem
  - Always an upgrade path (at a price!)

Bespoke MO –3 years / PXIe MO –6 months

D-LLRF : Staged implementation

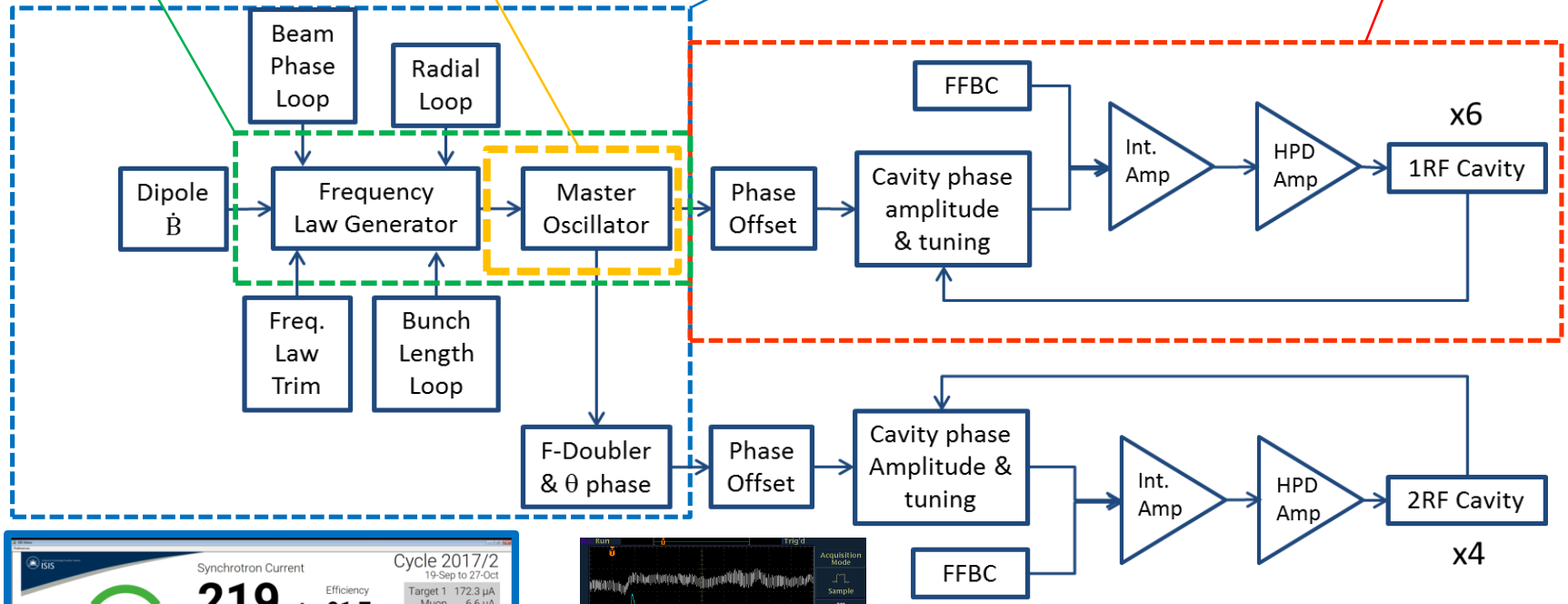
Aug 2014: Combined FLG / Digital Master Oscillator

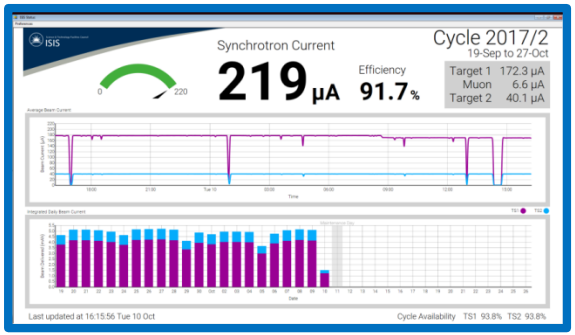
Dec 2013: Initial MO operation

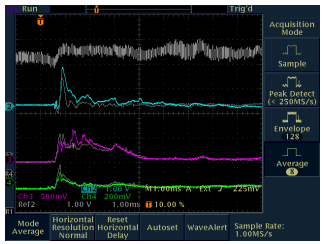
- Cavity RF generation, Frequency Doubler and Phase distribution
- Provides 1 x 1RF common Ref
- + 4 x 2RF Ref signals
- Operationally running in FPGA since February 2016

Digital IQ RF cavity loop control

- Initial tests Oct 2018
- 1x1RF cavity during user cycle June 2019
- 6x1RF cavities Sep 2019!







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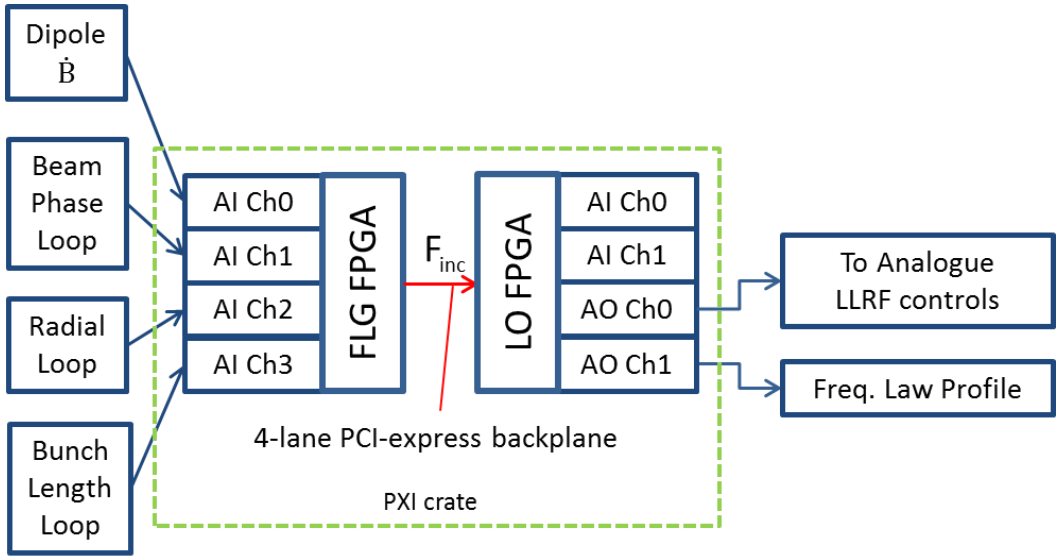
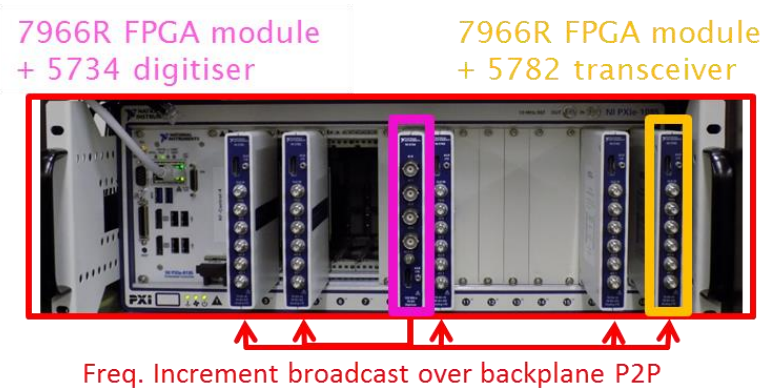
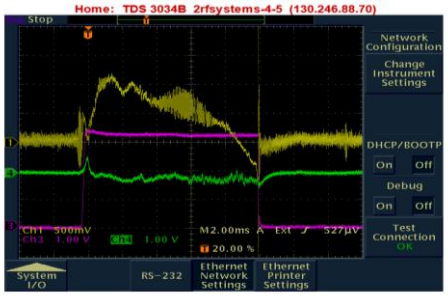
D-LLRF – Initial system design





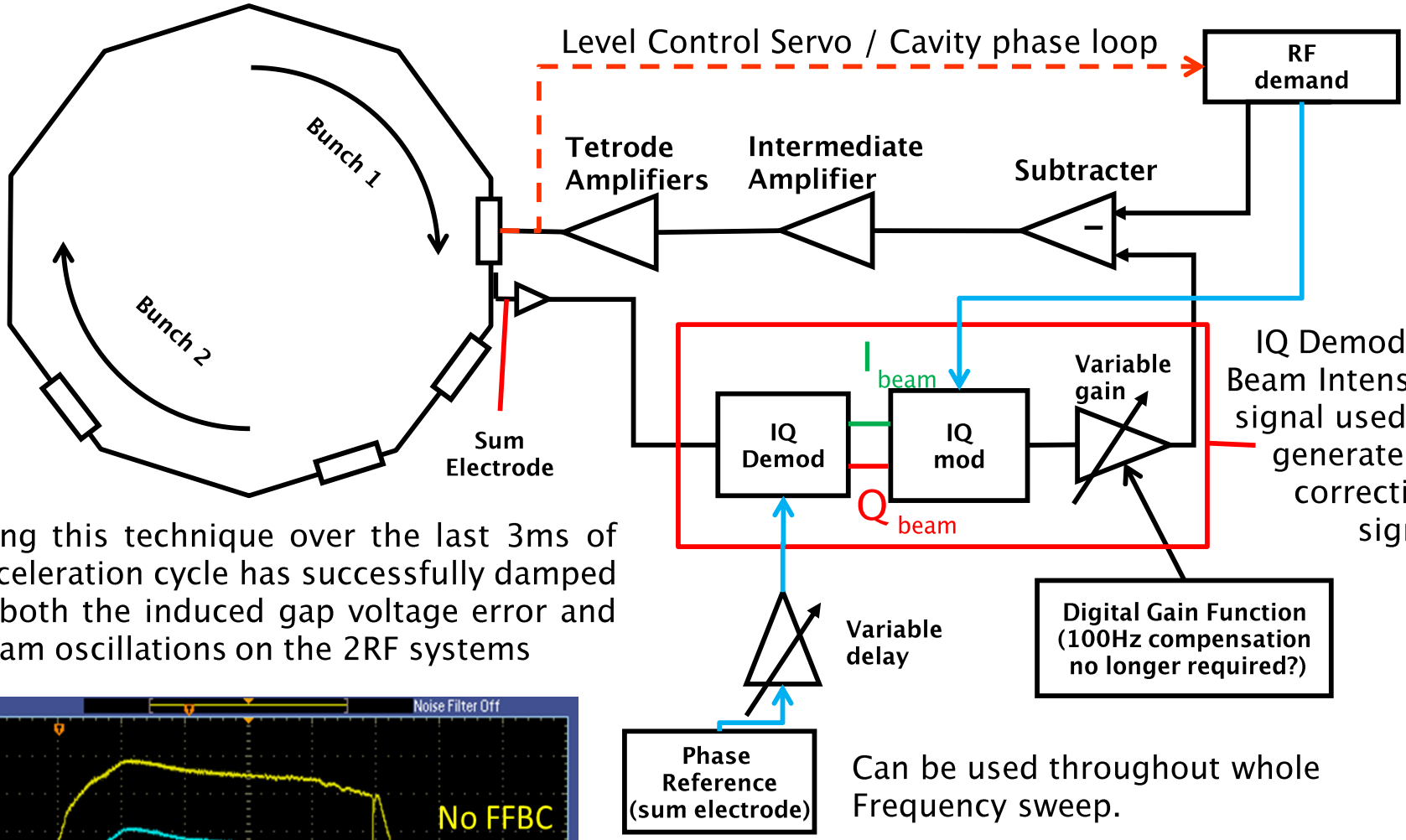
Worked well initially, for a single P2P link, but when used to close Beam Phase loop with design for more LOs, higher latency gave rise to catastrophic beam losses!



April 2015 code revised using PXI trigger lines for F-word broadcast rather than PCI express data stream

Other issues: loss of synchronisation over FPGA modules when running interactive mode. Cured by “Boot-up” exe RTOS deployment.

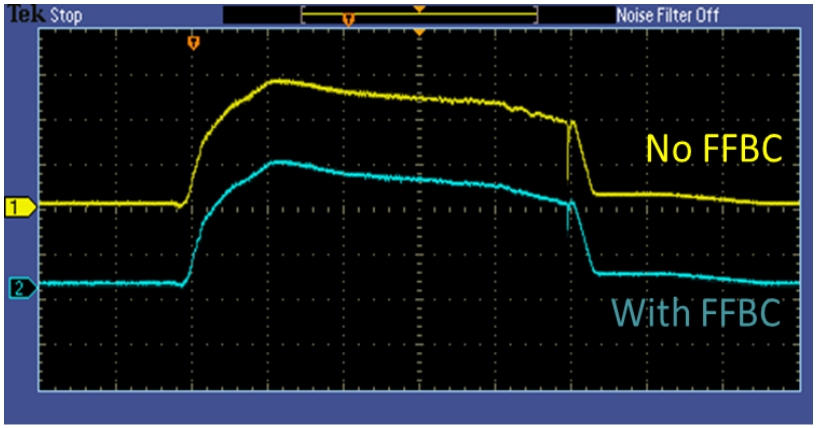
D-LLRF – IQ FeedForward Beam Compensation



IQ Demod of Beam Intensity signal used to generate FF correction signal

Applying this technique over the last 3ms of the acceleration cycle has successfully damped down both the induced gap voltage error and the beam oscillations on the 2RF systems

Can be used throughout whole Frequency sweep.



Accelerating Gap Voltage envelope

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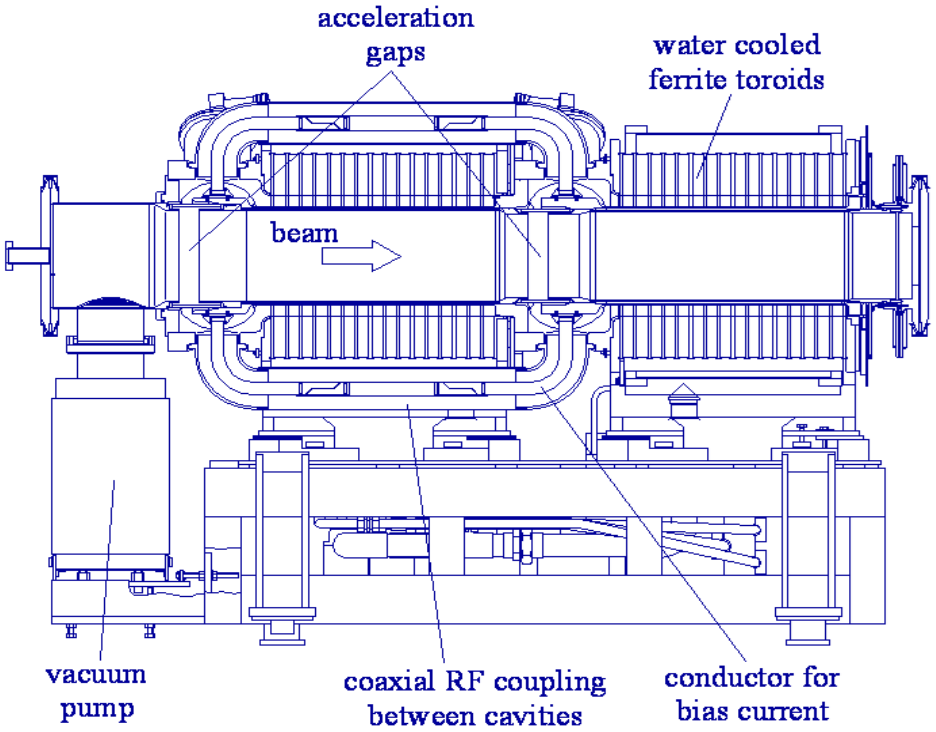
LLRF Cavity Tuning

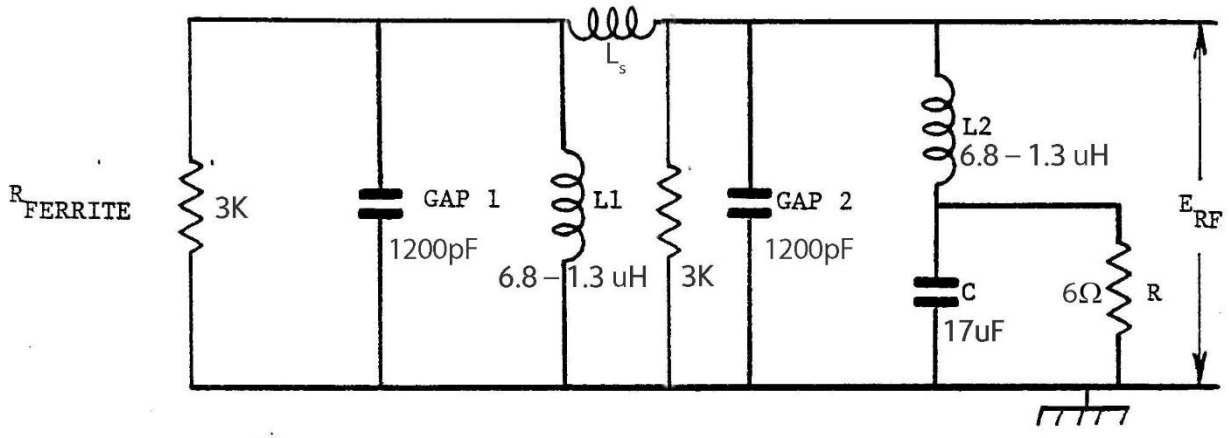


- RF fields are applied through cavity resonators

- The cavities must be tuned to resonate at the correct frequencies for acceleration

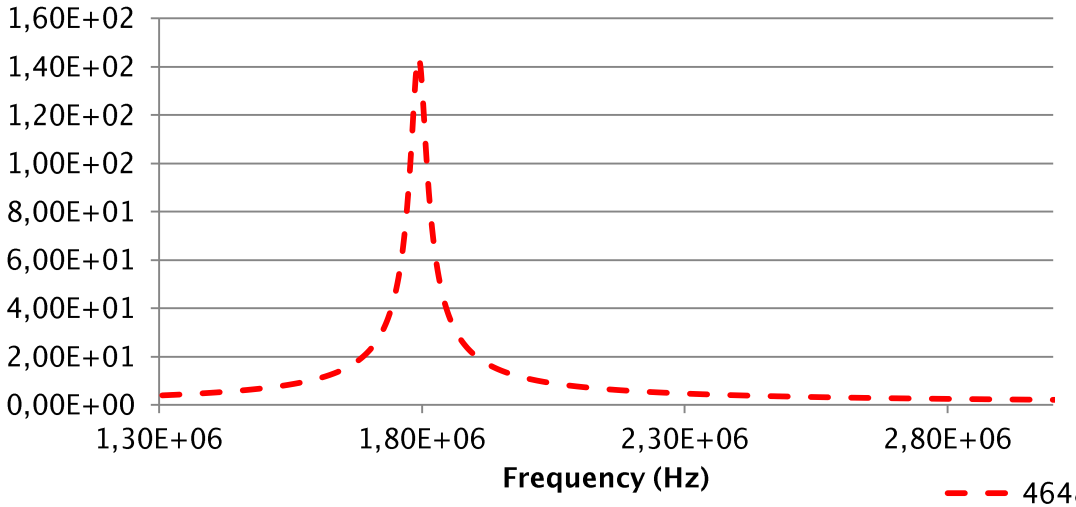
$$\omega_R = \frac{1}{\sqrt{LC}}$$

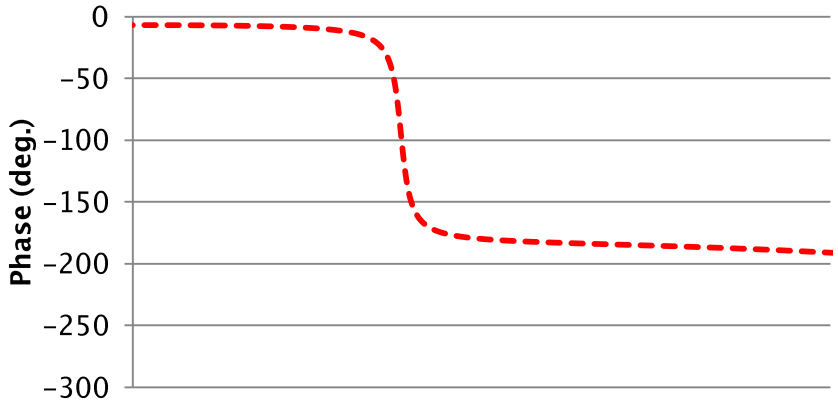
- ISIS cavities are tuned by altering the inductance of ferrite with a biasing field



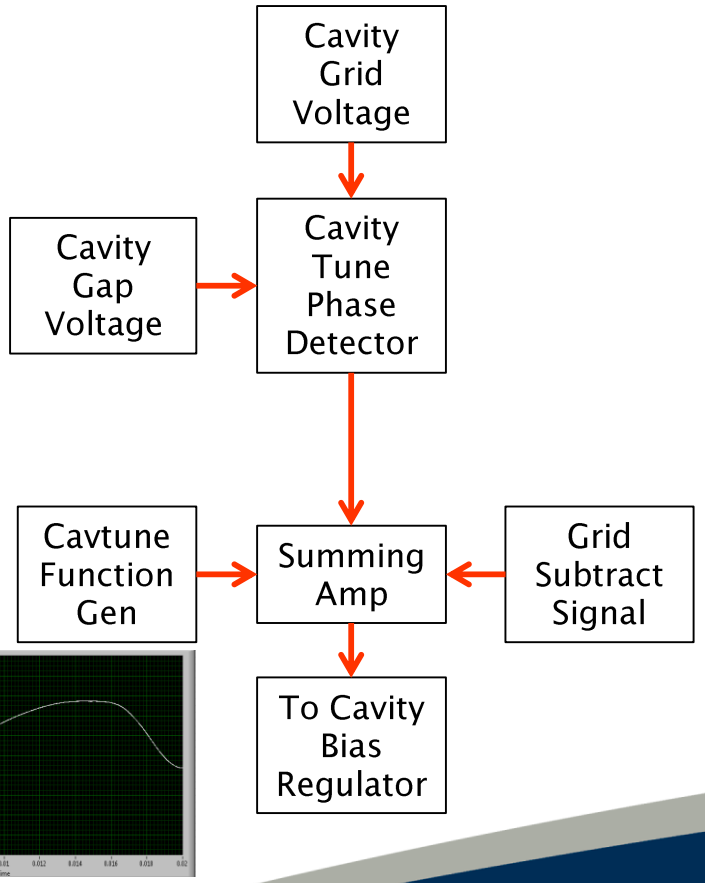
RF CAVITY CIRCUIT AS SEEN BY THE RF SUPPLY

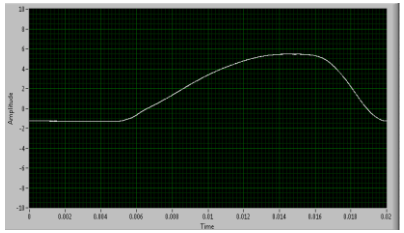
LLRF Cavity Tuning



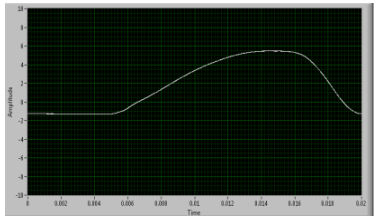


On resonance, cavity phase is -90 degrees wrt reference signal



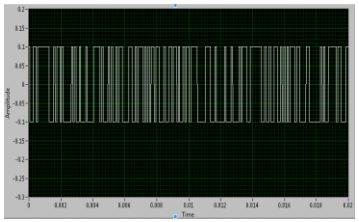


LLRF Cavity Tuning



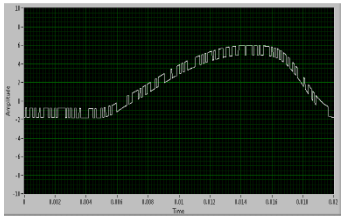
Tuning Demand Signal r(t)

+



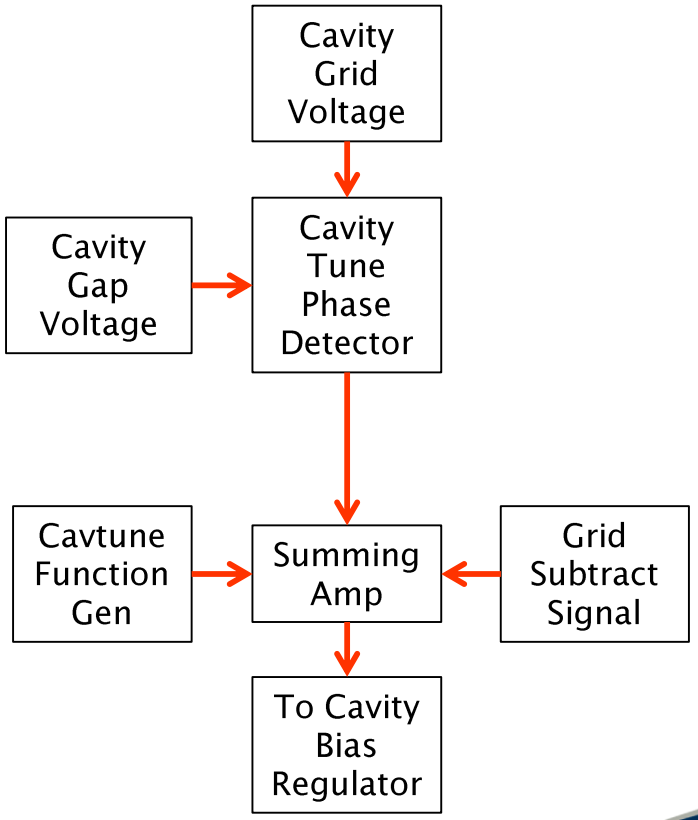
PRBS or Schroeder phased sinusoid

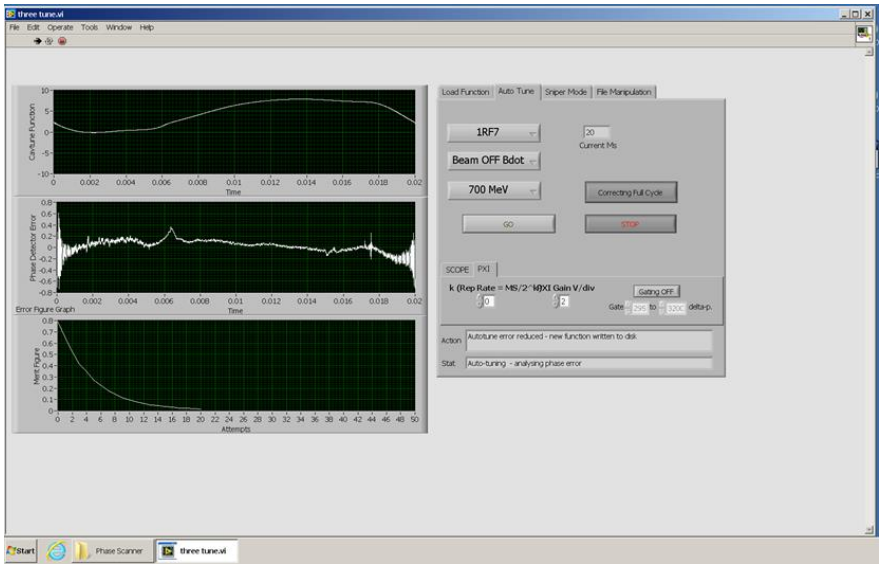
=



Known harmonic response of cavity tuning loop for each RF system

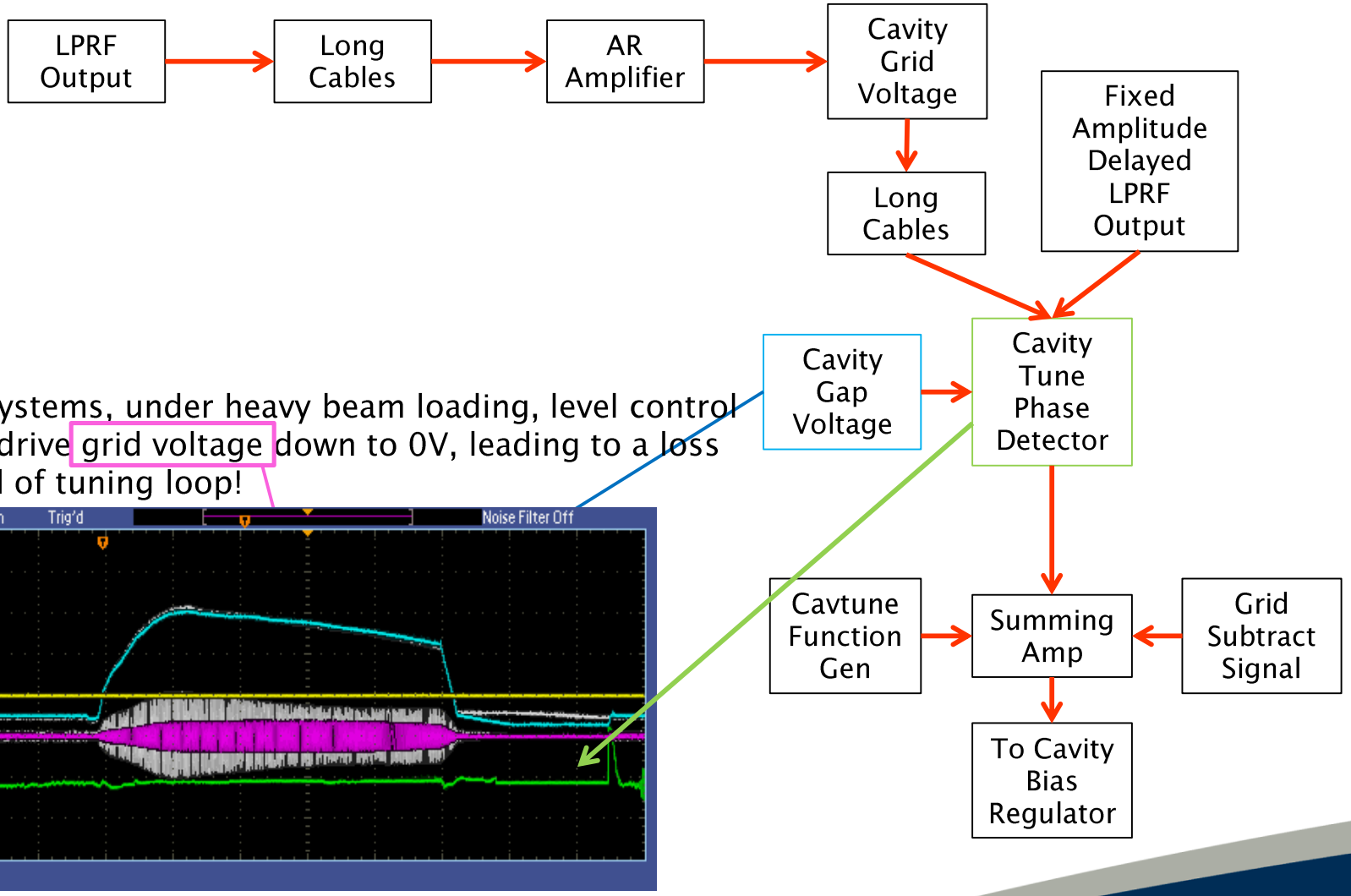
Cavtune Algorithm





Iterative routine to adjust the Bias function & minimise the tuning error

LLRF Cavity Tuning



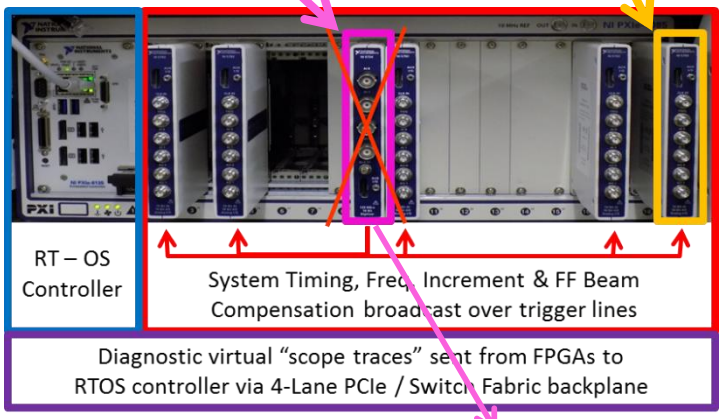
For 2RF systems, under heavy beam loading, level control loop can drive grid voltage down to 0V, leading to a loss of control of tuning loop!

Analogue version – successfully operating over last 2 years

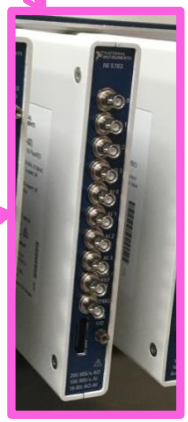
D-LLRF – System Architecture

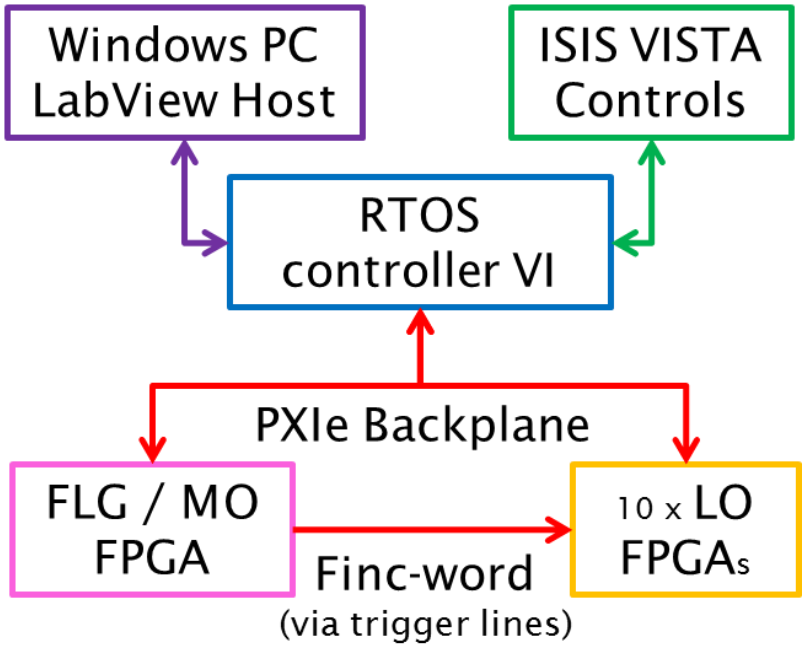
FLG / MO
7966R FPGA
module
+ 5734 digitiser

LO / IQ controller
7966R FPGA
module
+ 5782 transceiver



FLG / MO
7971R FPGA
module
+ 5783 transceiver





New FLG / MO
Bigger FPGA!
- Faster compiles

4 channel transceiver to give auxiliary outputs
- FL to intensity monitor
- RF for extract timing / beam choppers etc.

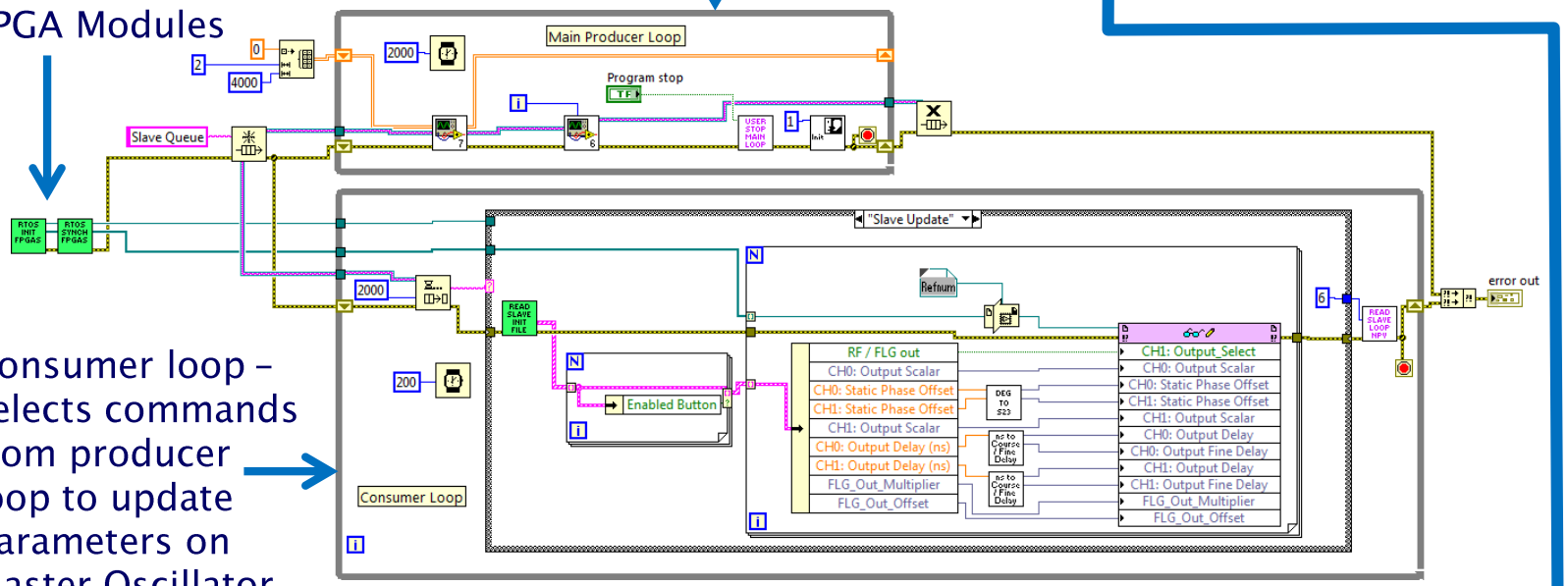
D-LLRF – System Architecture

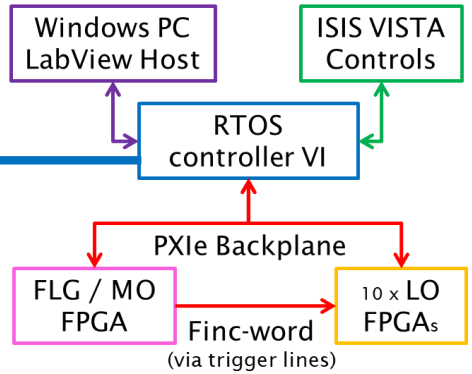
NI Realtime Controller

Boot-up executable file that downloads the bitfiles to each FPGA on power up, performs initialisation and clock synchronisation of the FPGA Modules

Producer loop- marshals commands from ISIS controls system and host VI program

Consumer loop – selects commands from producer loop to update parameters on Master Oscillator FPGA and each of the Local Oscillator FPGA Modules





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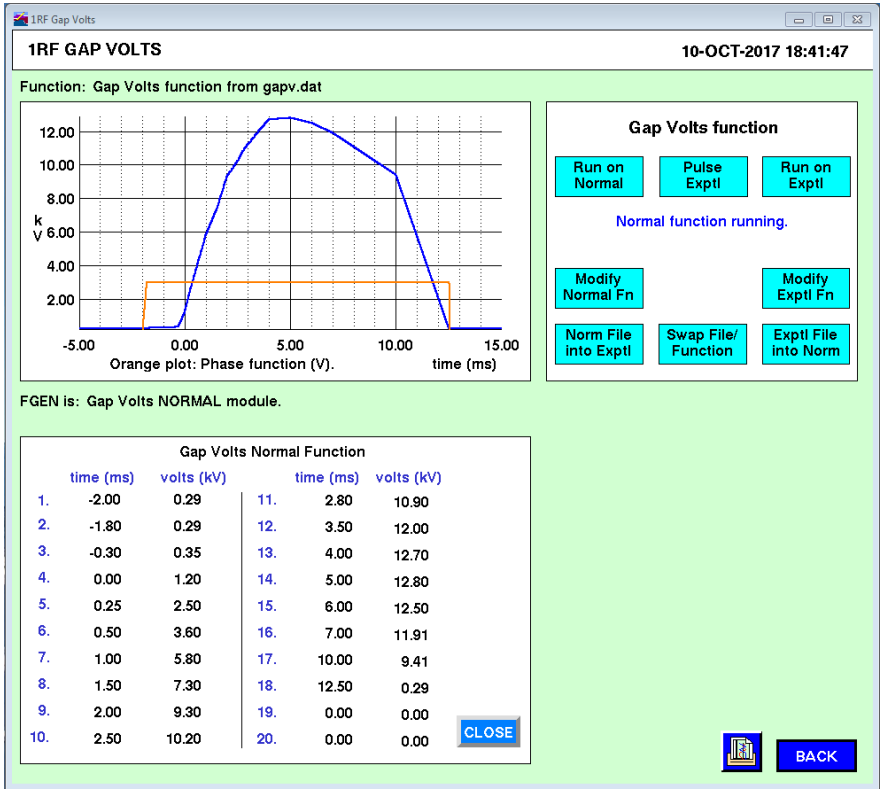
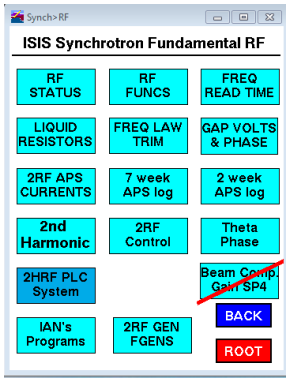
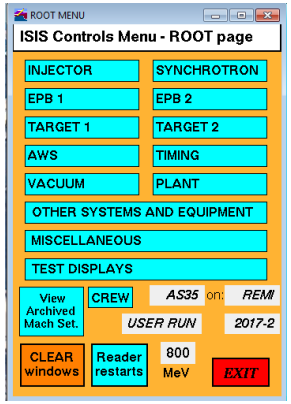
D-LLRF – System Architecture

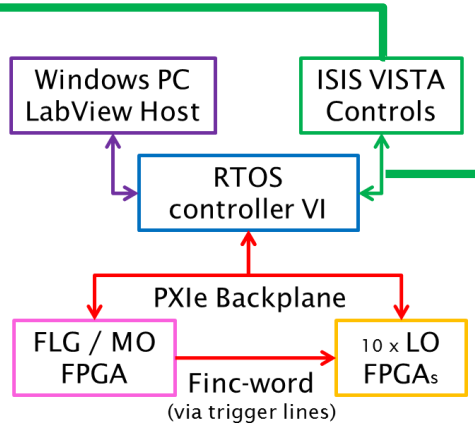
ISIS VISTA Controls system







ISIS Main Controls parameters set by machine operators



Now: PixyBroker

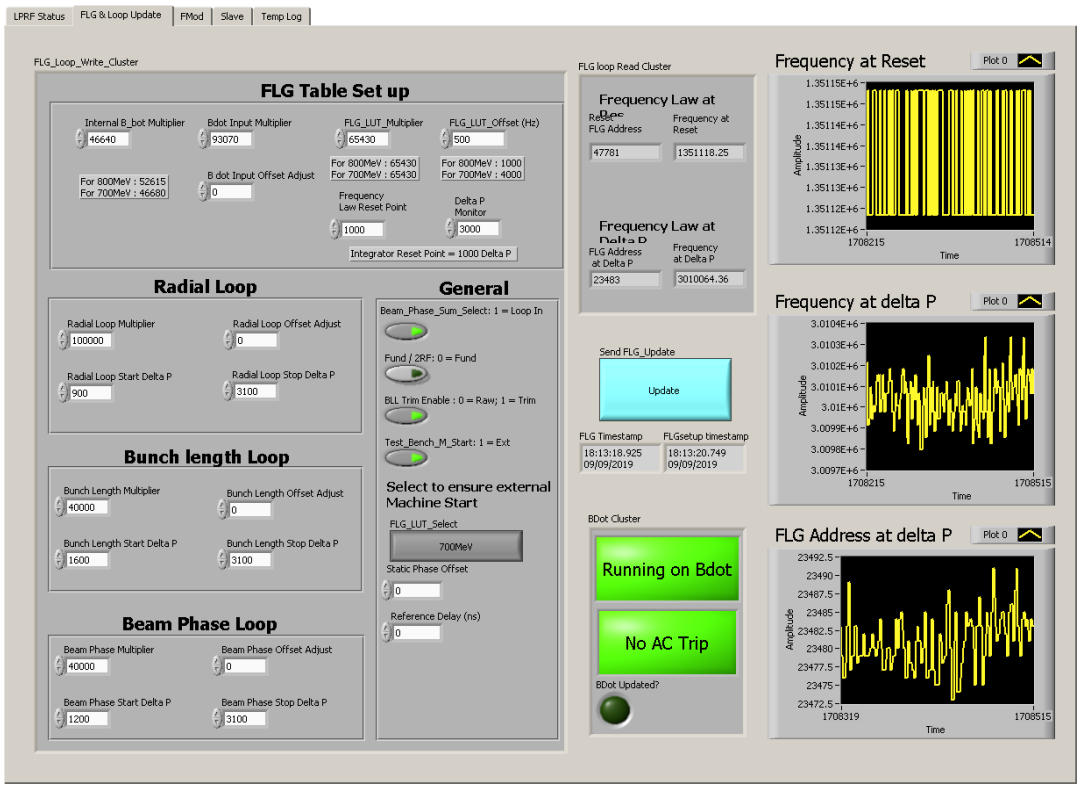
- LabView VI running on RTOS controller
- Polls Vista DB channel for changes every 2s

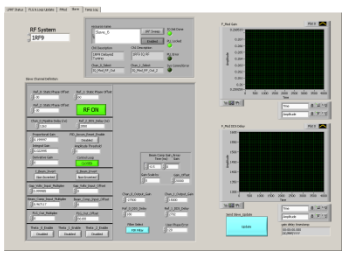
Soon: MQTT

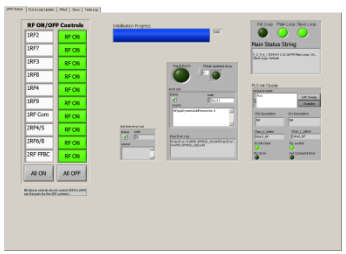
- MQTT is a Client Server publish/subscribe messaging transport protocol.
- Will include experimental function pulsing etc

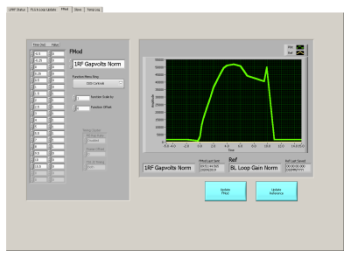
D-LLRF – System Architecture

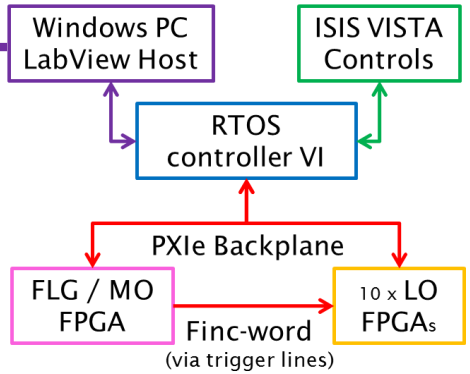
Windows PC diagnostics VI (RF Parameter setup)











Tabbed panes allow access to "Expert" parameter groups.

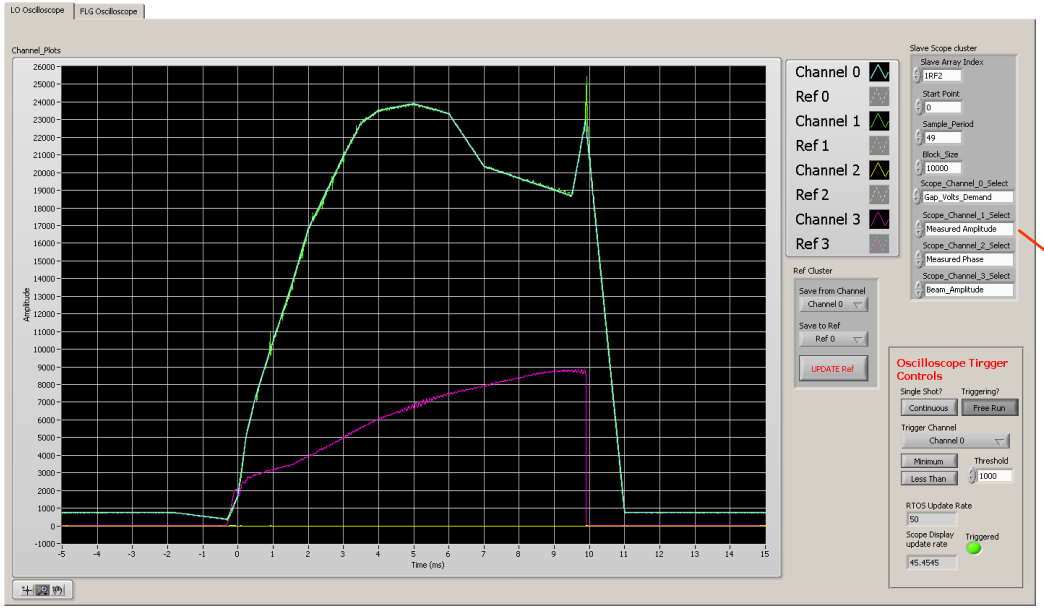
Now has simple LLRF On/Off buttons to replace analogue pots.

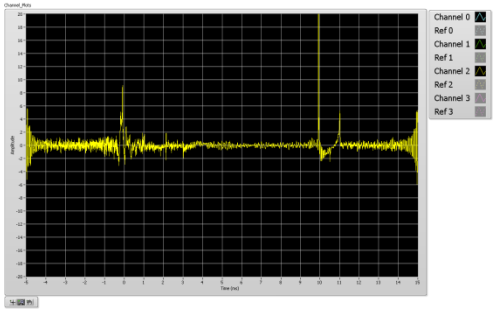
Allows interactive editing of RF setup parameters – phase offsets, Loop gains etc (set by RF team) and display of current values (eg start / stop frequency etc.)

Virtual "Function Module" channels show last sent values of VISTA controls functions.

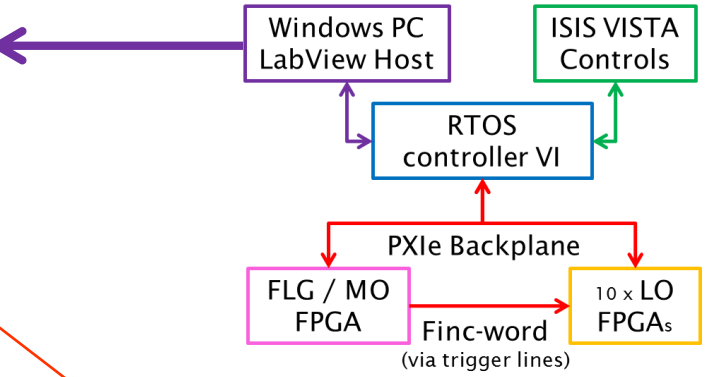
D-LLRF – System Architecture

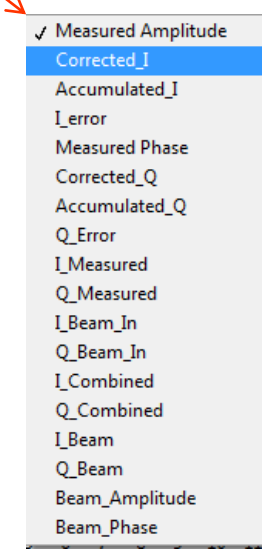
Windows PC diagnostics VI (Virtual scope traces)





Enables selection and display of test signals. Currently available for a selection of virtual test points in the FPGA code. Data streamed from each FPGA module to PXI controller via PCI-express back-plane and then to Host PC via Network Stream at up to 50Hz. Currently triggered by thresholding values on the receiver, but will soon be triggered at the FPGA.





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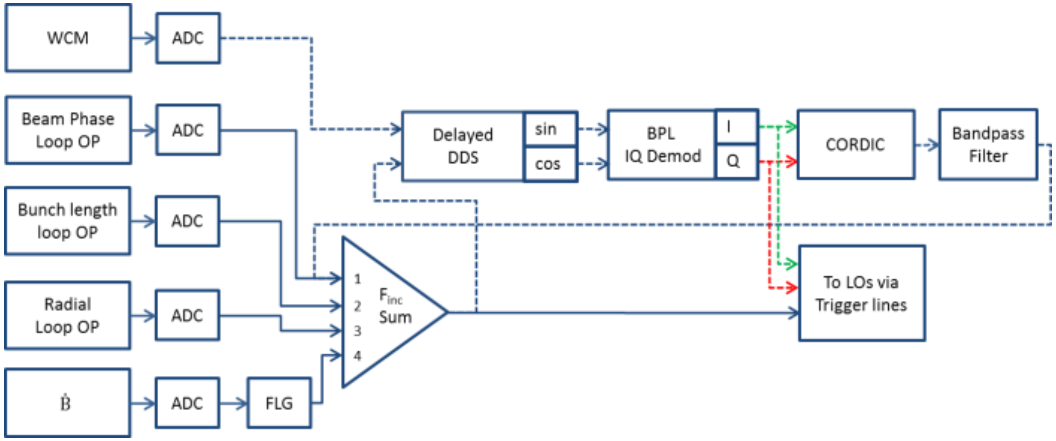
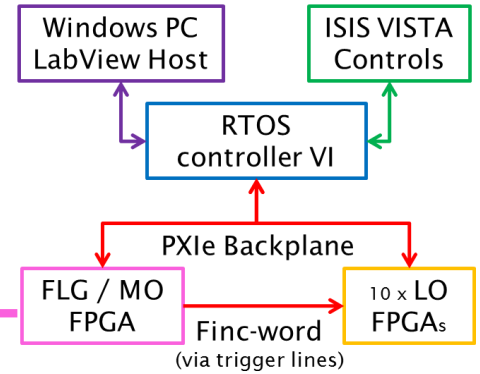
D-LLRF – System Architecture

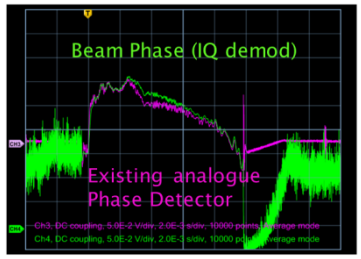
Frequency Law Generator / Master Oscillator

Implemented using LabView FPGA on NI PXIe7971R FPGA module + NI 5783 100MS/s transceiver adapter module generates the RF sweep from 1.3MHz to 3.1MHz for 1RF cavities and 2.6 to 6.3MHz for 2nd Harmonic cavities.



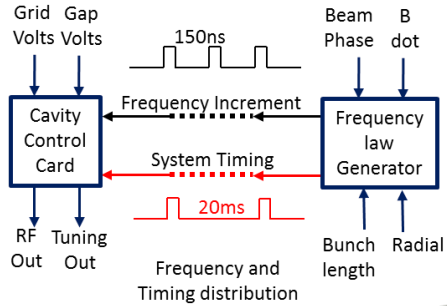


Currently using direct analogue loop inputs. Previous tests used IQ demodulation of the beam sum electrode signal followed by a CORDIC algorithm to generate a beam phase signal. This will be implemented to replace the existing analogue beam phase loop with the added benefit of using the same beam signal to generate the Bunch Length Loop correction (and possibly provide Beam I and Q for FFBC).



RF Synchronisation

Backplane trigger/data lines used for system timing, frequency increment broadcast and synchronous frequency update.



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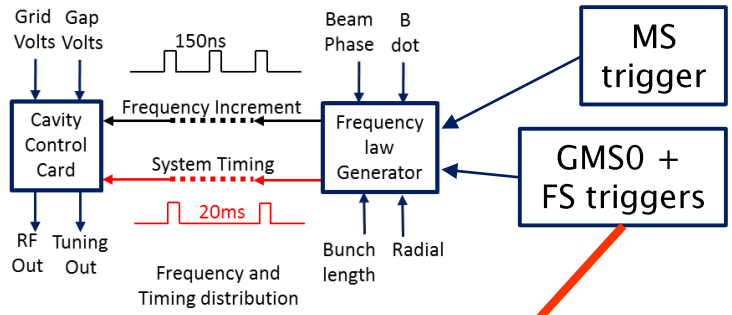
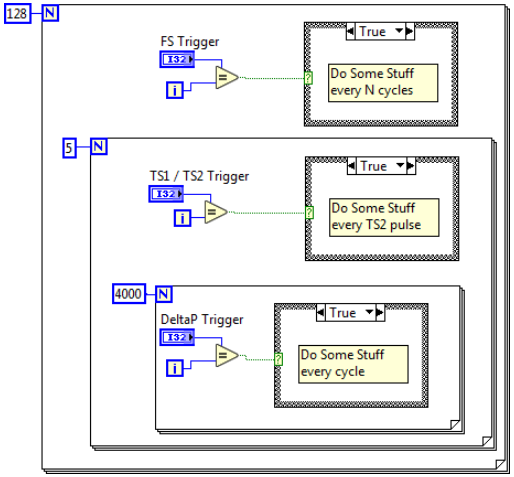
D-LLRF – ISIS Machine Timing

Replace MS trigger with FS trigger

- to allow pulsing Normal / experimental Functions at MS, MS/2, MS/4….MS/640.
- Includes possibility of applying different functions for TS1 / TS2 beam pulses.



LO counter



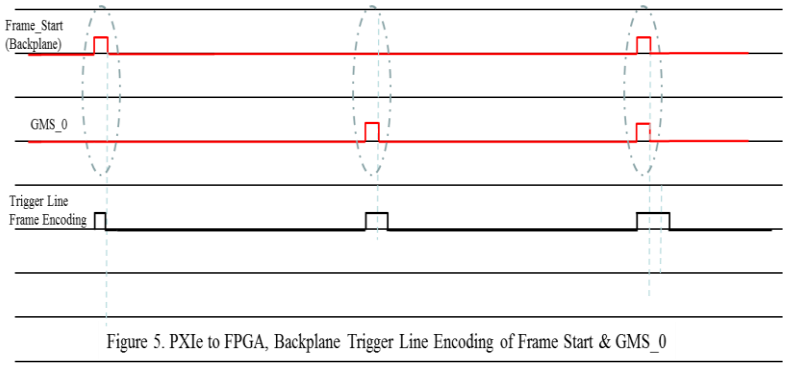
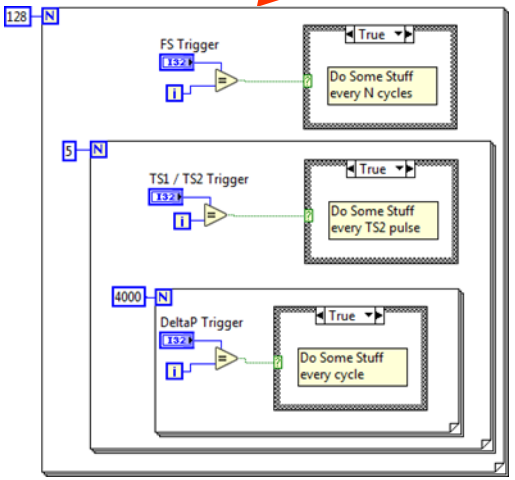


Figure 5. PXIe to FPGA, Backplane Trigger Line Encoding of Frame Start & GMS_0



FLG counter

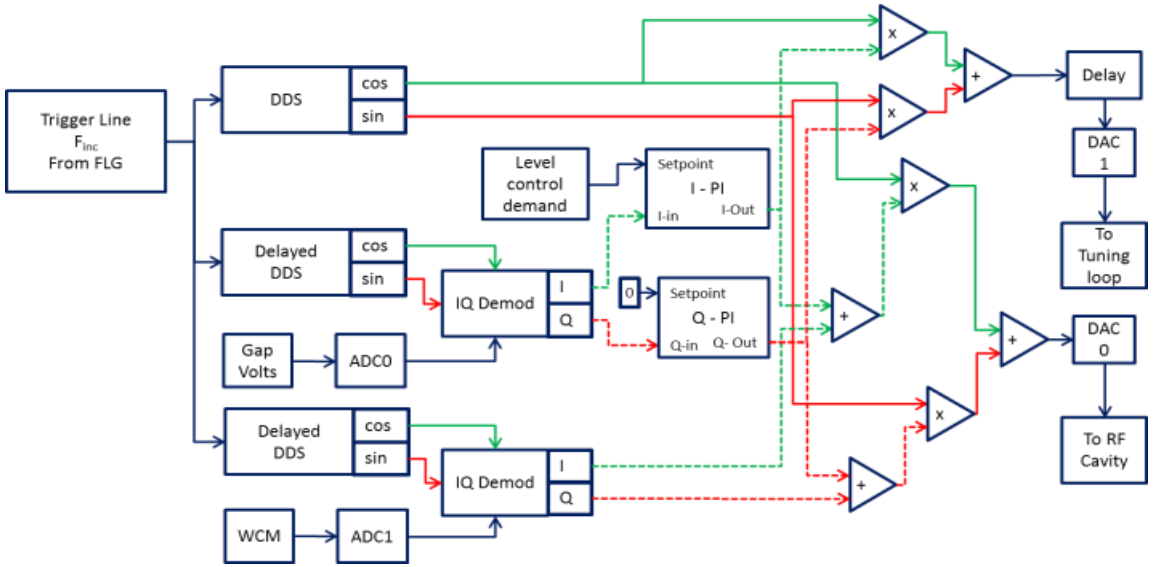
GMS 0 (or other external) triggering

- to allow switch off RF for non-beam pulses.

D-LLRF – System Architecture

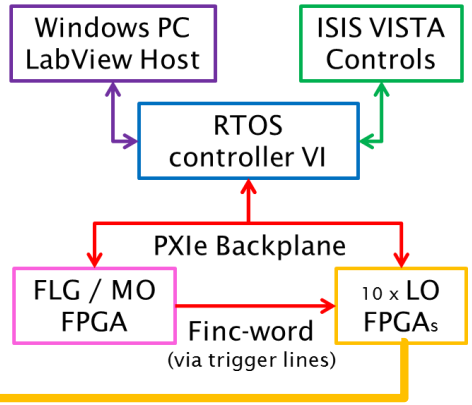
Local Oscillator

Implemented using LabView FPGA on NI PXIe7966R FPGA module (Virtex-5 SX95T FPGA /512 MB DRAM) + NI5782 250MS/s IF transceiver adapter module (6 x 1RF modules + 4 x 2RF Modules)



LO PID control loops

- Amplitude & Phase control on cavity using PI control loops for both I & Q vectors (10KHz Loop Response required)
- Will extend to Cavity tuning loop in the future (and have investigated use of reference signal to replace grid volts)



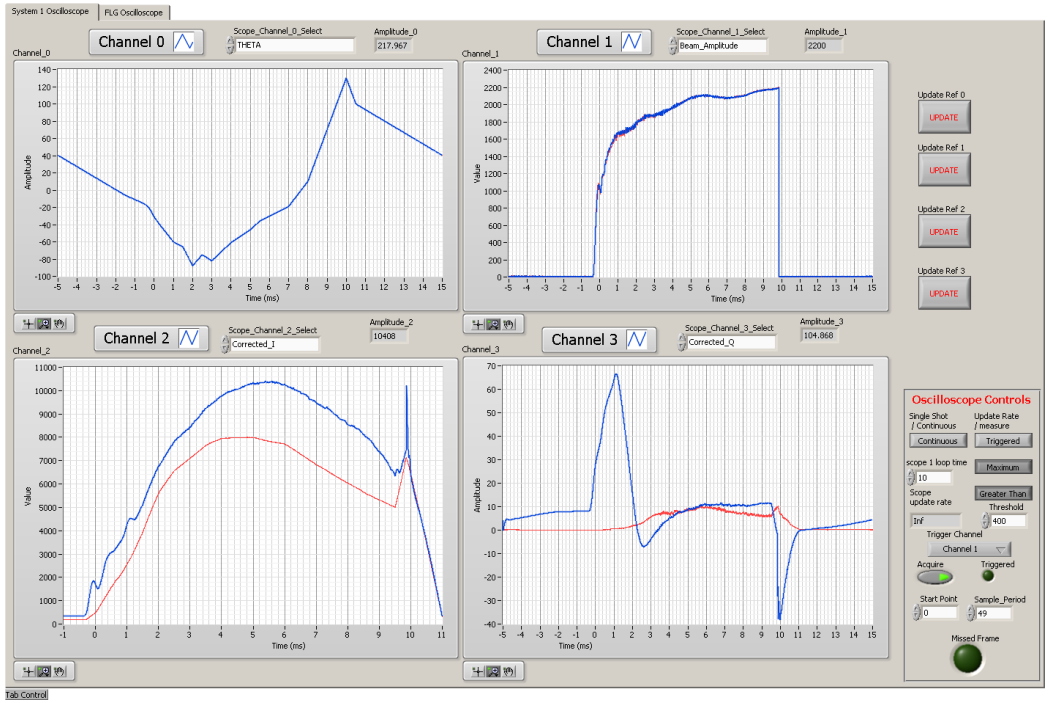
1.3-3.1MHz & 2.6-6.3MHz

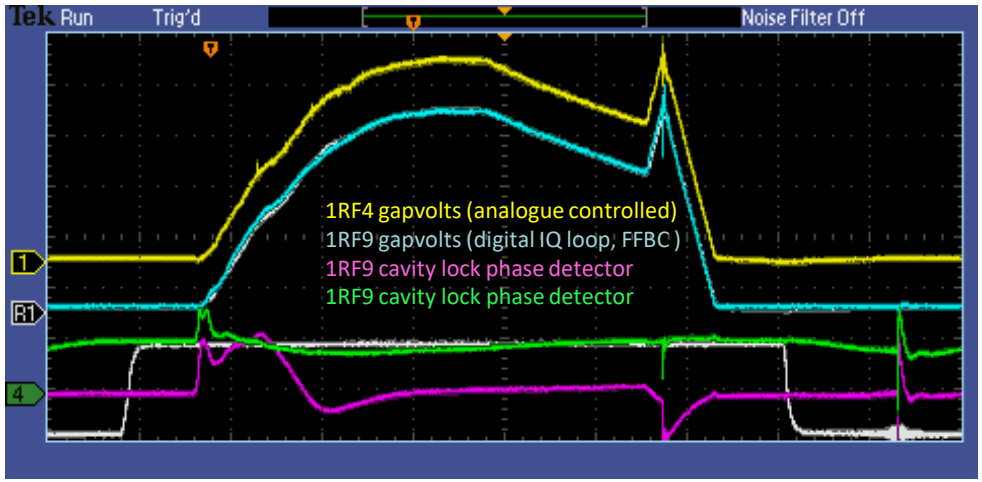
DIRECT SAMPLED!

1st iteration
I/Q ->CORDIC ->Amp/Phase loop

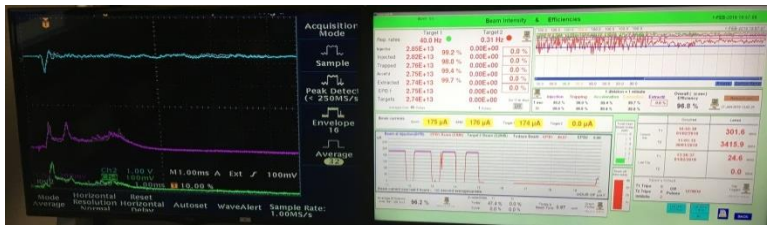
Now only as diagnostic

IQ Control Loop – tests





February / March 2019: Ran 40Hz Beam with digitally closed IQ loop on 1x 1RF system with High intensity beam and losses comparable to operational levels



No FF Beam Compensation applied (not possible at this beam intensity with the analogue system!)

Apparent improved Loop performance over Amplitude / phase loops – remove need for FFBC?

Without FFBC (or even with digital FFBC implemented in D-LPRF system if necessary) can retire old FFBC crates – source of high % of recent system outages

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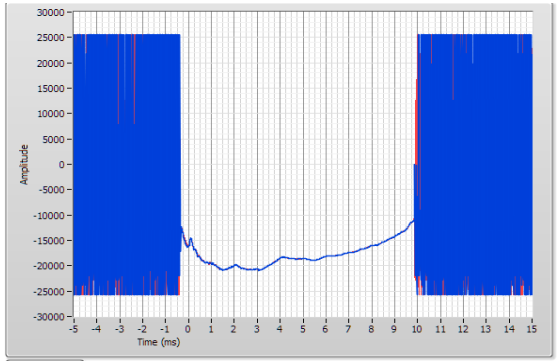
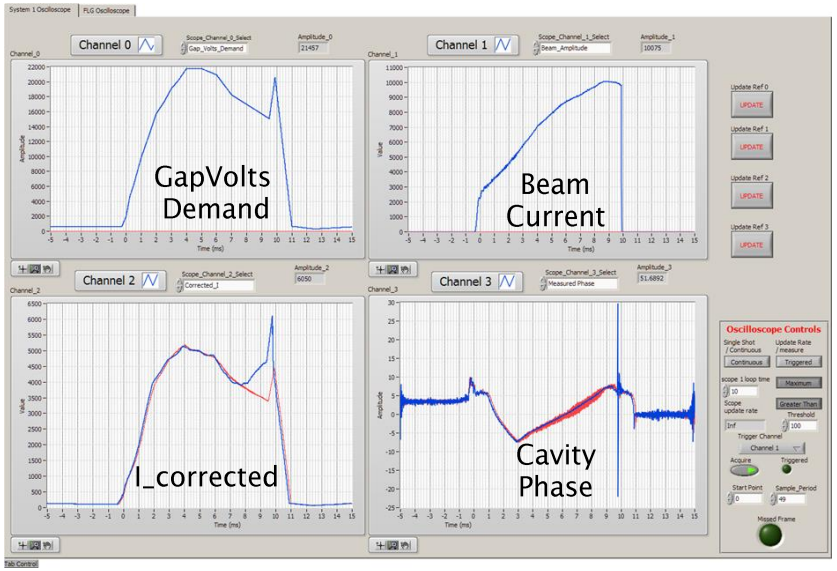
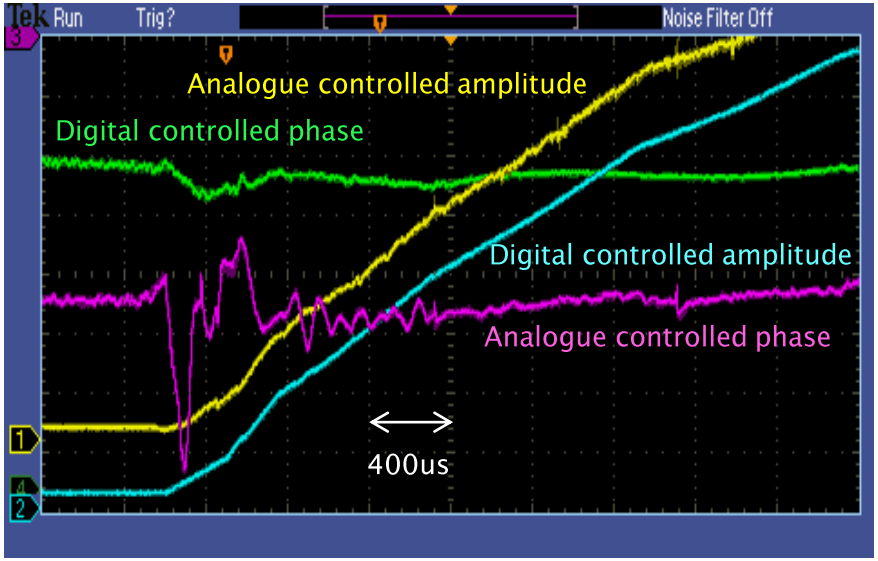
Digital FFBC – tests

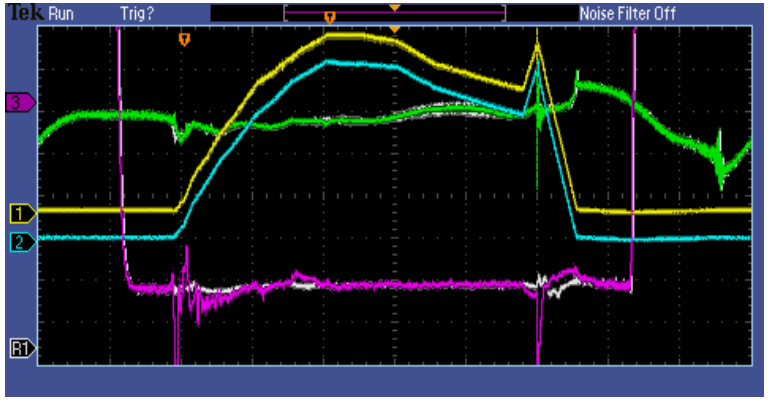
1. Set Beam IQ demod reference phase to match position of WCM
2. Adjust reference delay to give a reasonable beam phase from CORDIC





3. Adjust FFBC gain to match I_corrected to no beam case





Beam: 2.99e13 inj, 2.86e13 acc

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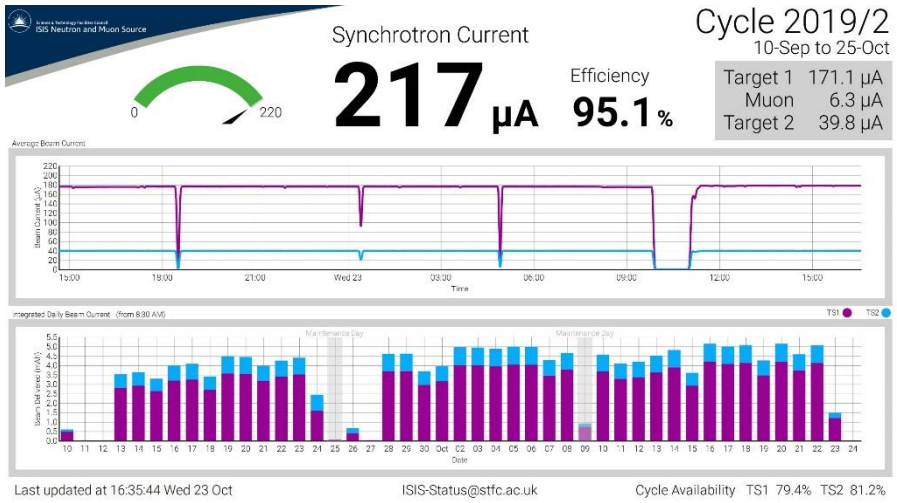
IQ Control Loop – Operation

Following success in the initial tests during machine development:

- Started the June ISIS user cycle running 1x1RF cavity with digital IQ loop control Had been running stably for ~1 week but ~3 hours into the User run, started to lose synchronisation between LO FPGAs
- Reverted to old FLG / MO FPGA and finished run in that state
- Subsequent investigations found differences in clock implementation on new 7971R FPGA module – leading to additional 2.5ns delay – Just sufficient to occasionally lose synch!
- Re-worked FLG/MO code to clock the F_{inc} bits at 20MHz (cf 40MHz previously)

ISIS User cycle 2019/2 (10th September – 25th October)

- Started cycle with 6x1RF cavities controlled with Digital IQ loops
- Problems with LINAC Tank 4 hampered beam setup – Limited time to configure so running on analogue FFBC system and old "Grid" tuning
- Will change tomorrow to delayed reference tuning and digital FFBC (or no FFBC) for next cycle



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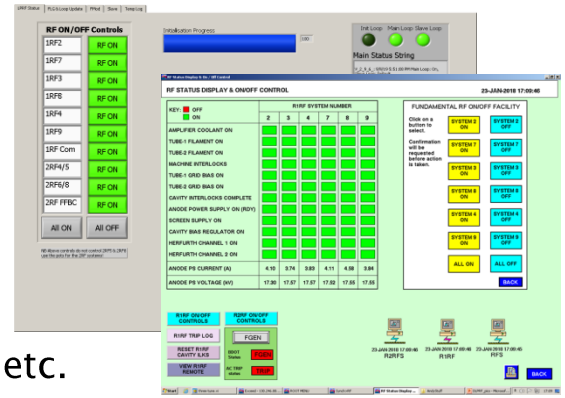
D-LPRF: still to do!



New MQTT based controls interface

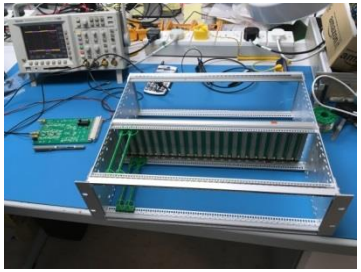
- Currently testing the code – seems to work well
- Integrate LPRF On/Off controls into ISIS controls pages

Update FLG / MO FPGA code

- Provide external RF sweep / triggering to extract timing etc.
- Implement Beam phase and bunch length Loops digitally
  Also gives Beam I / Q to send to LOs via trigger lines if required

Complete analogue buffer crates

- Final Design nearing completion
- 3U Eurocard standard
- Interface to NI front-end cards
- 24V High reliability Crate supply
- Implement IQ control of 2RF Cavities



Implement Cavity Tuning on LO FPGA

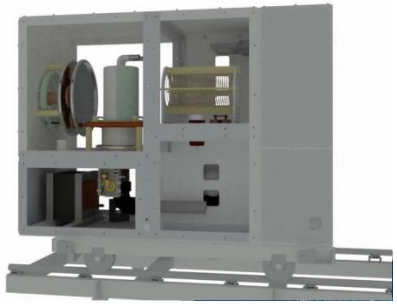
- Current utilisation ~ FLG: 50% cf LO: 90%
- May need more space: Implement FFBC IQ-demod on FLG / MO FPGA and broadcast over trigger lines

D-LLRF: the future

£  $

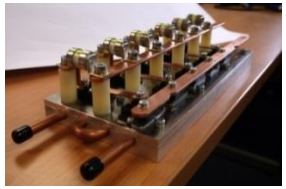
Investigate possible power saving

- GMS triggering Low or Zero Voltage RF demand for “no-beam” trigger (Trips / inhibits / downtime / shutdowns etc), and further reduce the RF electricity bill by 10-20%

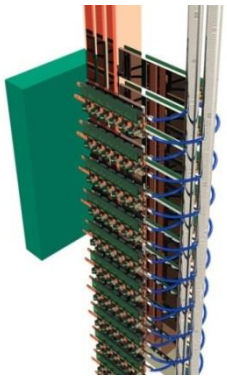


New High Power Drive Amplifiers

- Update for different cavity loading
- Is FFBC necessary?
- Different Tuning Requirements?

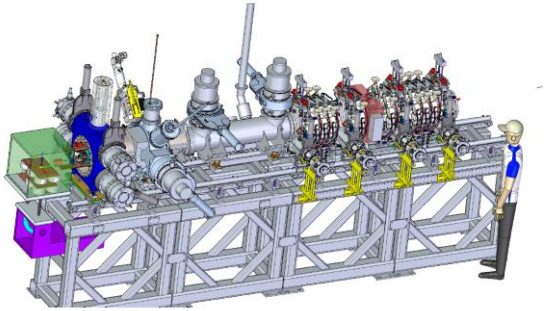


Update for tuning loop for new cavity bias system



Starting to look at working on FETS D-LLRF

- uses same NI FlexRIO hardware
- can re-use some of code eg Controls Interface, PI(D) loops
- FETS controls may run on EPICS? Can use this as a test bed for LabView / EPICS interface & then implement back into Synch D-LLRF
- Use above as a template for ISIS Pre-Injector LLRF upgrade



ISIS D-LLRF – Summary

ISIS LLRF not a greenfield site

- Staged implementation – must be easily "Undo-able"
- Code snippets tested during limited machine development time (eg IQ beam phase, D-FFBC)
- Initial basic operation – overcame initial mistrust of PXI platform from machine operators

Off the shelf hardware sped up initial development time

- But needed hefty code workarounds for backplane latency, synch issues etc.

IQ operation

- IQ loop out-performs previous Amplitude/Phase loops with beam
  For ~2.5e13 protons old analogue system would lose phase lock and lose the beam!
- Digital FFBC – even if required will still enable ageing analogue units to retire

Lots of re-usable code modules for other LPRF projects

Running the Current User Cycle with 6x1RF controlled with digital IQ loops

Soon Full Digital Control all 10 cavities!

Thank you!